6
Strained Silicon Nanodevices

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6.1
Introduction

The history of solid-state devices began with the invention of the transistor by Bardeen, Brattain, and Shockley in 1947 [1]. Only a few years later, the first integrated circuits were realized by Texas Instruments (1958) and Fairchild Camera in 1961, assigning the first stages of the development of the microelectronics industry. Since its inception, the industry has experienced five decades of unprecedented explosive growth driven by two factors: Noyce and Kilby inventing the planar integrated circuit [2, 3] and the advantageous characteristics that result from scaling (shrinking) solid-state devices. Scaling devices have the peculiar property of improving cost, performance, and power. As a result, the microelectronics industry has driven transistor feature size scaling from 10 μm to about 30 nm during the past 40 years. However, starting with 90 nm technologies, the performance enhancements of complementary metal–oxide–semiconductor (CMOS) devices started to diminish through standard device scaling such as shrinking the gate length and thinning the gate oxide due to several physical limitations in miniaturization of metal–oxide–semiconductor field-effect transistors (MOSFETs). For example, thinning the gate oxide requires a reduction in the supply voltage and an increase in the gate tunneling current occurs. Furthermore, raising the dopant concentration in the substrate is substantial to suppress short-channel effects that decrease both the carrier mobility and the drive current.

Thus, new channel structures and materials, which mitigate the stringent constraints regarding the device design, have recently stirred a strong interest. These so-called *technology boosters* [4] include strained silicon channels, ultrathin silicon on insulator (SOI), metal gate electrodes, multigate structures, ballistic transport channels, and others. Among them, strained silicon channels have been recognized as a technology applicable to near term technology nodes [5–7]. The mobility enhancement obtained by applying appropriate strain provides higher carrier velocity in MOS channels and drive current, respectively, at the same supply voltage and gate

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oxide thickness. It implies that thicker gate oxides and lower supply voltage need to be used for a fixed drive current, leading to the mitigation of the trade-off relationship among drive current, power consumption, and short-channel effects.

6.2 Impact of Strain on the Electronic Properties of Silicon

The change of the electrical resistance of a material due to applied stress is generally known as piezoresistive effect. In electrodynamics, this is expressed by the material equation

$$\hat{J} = \hat{\sigma} \cdot \hat{E} \tag{6.1}$$

where $\hat{J}$ is the tensor of the current density and $\hat{E}$ is the tensor of the electric field. Applying mechanical stress results in a dependence of the conductivity tensor $\hat{\sigma}$ on the tensor of mechanical stress. The components σ_{ij} of the conductivity tensor can be written as [8]

$$\sigma_{ij} = -\frac{e^2}{4\pi^3} \int \frac{\partial f_0(\varepsilon)}{\partial \varepsilon} \tau(\varepsilon) \vartheta_i \vartheta_j \mathrm{d}^3\vec{k}, \quad i,j \in \{x,y,z\} \tag{6.2}$$

Here e is the electron charge, $\vartheta_i = \bar{h}^{-1} \partial\varepsilon(\vec{k},\hat{X})/\partial k_i$ is the ith component of the group velocity of charge carriers, ε is the carrier energy, $\vec{k}$ is the wave vector, $\hat{X}$ is the elastic stress tensor, f_0 is the equilibrium distribution function, and τ is the relaxation time. At $\varepsilon = \varepsilon_o(\vec{k})$, Eq. (6.2) describes the conductivity of the unstrained silicon. If strain is applied, that is, the energy of the free carriers receives some additional $\Delta\varepsilon$, which is a function of the wave vector $\vec{k}$ and the stress tensor $\hat{X}$,

$$\varepsilon = \varepsilon(\vec{k}) + \Delta\varepsilon(\vec{k},\hat{X}) \tag{6.3}$$

then the linear addition of the components of the conductivity tensor is [8, 9]

$$\begin{aligned} \sigma_{i,j} &= -\frac{e^2}{4\pi^3} \int \Delta \left[\tau(\varepsilon) \frac{\partial f_0(\varepsilon)}{\partial \varepsilon} \vartheta_i \vartheta_j \right] \mathrm{d}^3\vec{k} \\ &= -\frac{e^2}{4\pi^3} \left\{ \int \Delta\varepsilon \frac{\partial}{\partial \varepsilon} \left[\tau(\varepsilon) \frac{\partial f_0(\varepsilon)}{\partial \varepsilon} \vartheta_i \vartheta_j \right] \vartheta_i \vartheta_j \mathrm{d}^3\vec{k} + 1\bar{h} \int \tau(\varepsilon) \frac{\partial j_0(\varepsilon)}{\partial \varepsilon} \left[\frac{\partial \Delta\varepsilon}{\partial k_i} \vartheta_j + \frac{\partial \Delta\varepsilon}{\partial k_j} \vartheta_i \right] \mathrm{d}^3\vec{k} \right\} \end{aligned} \tag{6.4}$$

Using the first-order piezoresistance coefficients determined by the relation [10]

$$\pi_{ijkl} = -\frac{1}{\sigma_{ij}(\hat{X}=0)} \frac{\partial \sigma_{ij}(\hat{X})}{\partial X_{kl}} \bigg|_{(\hat{X}=0)}, \quad i,j,k,l \in \{x,y,z\} \tag{6.5}$$

the conductivity tensor for silicon could be written as [8]

$$\sigma_{ij}(\hat{X}) = \sigma_0 (\delta_{ij} - \textstyle\sum_{kl} \pi_{ijkl} X_{kl}) \tag{6.6}$$

with δ_{ij} as the Kronecker delta. Caused by the cubic symmetry of silicon (space group $m3m$), the fundamental coefficients of the piezoresistance tensor are reduced to 3, that is,

$$\pi_{11} \equiv \pi_{xxxx}, \quad \pi_{12} = \pi_{xxyy} = \pi_{yyxx}, \quad \pi_{44} \equiv 2\pi_{xyxy}$$

where π_{11} are the longitudinal (current and field are in the direction of the strain), π_{12} the transverse (current and field are perpendicular to the strain direction), and π_{44} the shear piezoresistance coefficients.

The piezoresistance coefficients of silicon and germanium were measured for the first time by Smith [11] in 1954. The data are valid only for bulk material and are widely applied to configure micromechanical elements such as pressure sensors [12]. For devices such as MOSFETs, however, surface confinement effects must be taken into account. Coleman *et al.* [13] measured the π-coefficients in p-type inversion layers for (100), (110), and (111) surface orientations. More recently, Chu *et al.* [14] published data for π-coefficients for n- and p-type silicon with different surface orientation and channel directions. It was shown that the π-coefficients are significantly different from the bulk values if surface confinement effects are regarded. The coefficients strongly depend on doping density, electric field, and channel direction even for nMOSFETs on (100) surfaces. The dependence of the π-coefficients on the channel length of MOSFETs prepared on SOI material was studied by Chang and Lin [15] for $\langle 110 \rangle$-oriented, submicrometer n- and p-type channels on (100) substrates.

In the presence of strain in a cubic semiconductor, the reduced degree of symmetry gives rise to significant changes in the band structure. Based on group theory and **k–p** perturbation calculations, several theoretical investigations have been carried out on the valence and conduction bands in silicon. Most of these investigations are based on the deformation potential theory. In this theory, the effect of the deformation is represented by the deformation potential Hamiltonian H_{DP}, which is linear in the components of the strain tensor. To calculate the change of the band structure, H_{DP} is usually treated as a small perturbation. A more generalized formulation for homogeneous strain is the *Pikus–Bir Hamiltonian* [9]. The deformation potential theory was originally developed by Bardeen and Shockley in 1950 [16] to calculate the components of the relaxation time tensor in terms of the effective mass, elastic constants, and a set of deformation potential constants. The deformation potential theory was generalized by Herring and Vogt [17] to model carrier transport in strained multivalley semiconductors and summarized a set of independent deformation potentials to characterize the conduction band valleys. The deformation potentials describe the shifts of the extremum energy of a particular valley depending on the magnitude of stress and its direction with respect to the $\vec{k}$ vector of the valley. The original model of Herring and Vogt was refined over the last decades. Balslev [18] determined the dilatation (Ξ_{d}) and shear deformation potential constants Ξ_{u}. The author also measured the deformation potentials a, b, and d defined by Ref. [9], characterizing the effect of strain on the valence band edge. While Balslev described the deformation potentials in the case of uniaxial strain, Hinckley and Singh [19]

assigned deformation potentials for biaxially strained layers. Furthermore, Nakayama [20] modified the theory of Herring and Vogt in combination with the results of Pikus and Bir (compare Ref. [9]) for stronger deformation, where the periodicity of the deformed crystal is different from that of the initial, undeformed state and the ordinary perturbation theory cannot be applied. Deformation potentials are applied in current models of the effects of uniaxial or biaxial strain on the band structure of silicon and the consequences on the electron and hole mobility [21–23].

The effect of strain on the band structure of silicon and on the carrier mobility takes place mainly due to

(a) the reduction of the carrier conductivity effective mass, and
(b) the reduction in the intervalley phonon scattering rates.

The conduction band of unstrained bulk silicon has six equivalent valleys along the $\langle 100 \rangle$ direction of the Brilloun zone, and the constant energy surface is ellipsoidal with the transverse effective mass $m_t = 0.19\ m_0$ and the longitudinal effective mass $m_l = 0.916\ m_0$ [24]. In the inversion layer on a (100) surface, these six valleys are split into twofold degenerate valleys with m_l perpendicular to the Si/SiO_2 interface and the fourfold degenerate in-plane valleys with m_t. If strain is applied, the energy of the conduction band minima of the fourfold valleys on the in-plane $\langle 100 \rangle$ axes rises with respect to the energy of the twofold valleys on the $\langle 100 \rangle$ axes perpendicular to the plane. As a consequence, the electrons prefer to populate the lower valleys, which are energetically favored. This result in an increased electron mobility via a reduced in-plane and an increased out-of-plane electron conductivity mass. Numerical simulations of the increased electron mobility were done using the Kubo–Greenwood formula for mobility, which are in good agreement with the experimentally measured data [25]. For a given strain, quantifying the effective mass reduction and comparing it to the enhanced mobility reveals that mass reduction alone explains only part of the mobility enhancement. Vogelsang and Hofmann [26] first suggest that the suppression of intervalley scattering rate is also important. Electron scattering is reduced due to the conduction valleys splitting into two sets of energy levels, which lowers the rate of intervalley phonon scattering. The effect of phonon scattering on the relaxation time τ was discussed by Fischetti and Laux [21]. Both types of scattering (acoustic and optical phonons) as well as their dependence on the density of states (DOS) in each valley were considered. The effect of the different scattering mechanisms depends on the strength of the electric field. Optical phonon scattering dominates at higher electric fields, while Coulomb, surface roughness, and acoustic phonon scattering are significant for low electric fields.

Many types of strain increase the electron mobility such as in-plane biaxial and uniaxial tensile and out-of-plane uniaxial compressive strain. Uchida *et al.* [27] first described the effect of biaxial and uniaxial strains parallel to $\langle 100 \rangle$ and $\langle 110 \rangle$, respectively, on the electron mobility and their behavior on the electrical performance of MOSFETs. It was shown that lower uniaxial strain parallel to $\langle 110 \rangle$ results in a larger enhancement of the electron mobility than the biaxial strain.

For holes, the valence band structure of silicon is more complex than the conduction band. Hasegawa [28] as well as Hensel and Feher [29] used band

structure calculations to systematically study the valence band effective masses and deformation potentials in strained silicon. They revealed that the hole mobility is mainly affected by band splitting and warping, mass change, and consequently by changes of the DOS, which alters band occupation and phonon scattering. A theoretical description of the hole mobility enhancement by strain was recently published by Fischetti *et al.* [30] using $\mathbf{k}\cdot\mathbf{p}$ perturbation calculations. The band warping is responsible for the fact that different types of strain (biaxial tensile and uniaxial compressive) behave differently. For unstrained silicon at room temperature, holes occupy the top two bands: heavy and light hole bands [30]. Applying strain, the hole effective mass becomes highly anisotropic due to band warping and the energy levels become mixtures of the pure heavy, light, and split-off bands. Thus, the light and heavy hole bands lose their meaning, and holes increasingly occupy the top band at higher strain due to the energy splitting. Important to achieving high hole mobility is a low in-plane conductivity mass for the top band. In addition to a low in-plane mass, a high density of states in the top band and a sufficient band splitting to populate the top band are also required. Uniaxial compressive strain on both (100) and (110) surfaces, for instance, create a high density of states in the plane of the MOSFETs.

6.3 Methods to Generate Strain in Silicon Devices

6.3.1 Substrates for Nanoscale CMOS Technologies

There are generally two different methods to introduce strain in the channel region: biaxial strain and uniaxial strain. Biaxial strain is also referred to as global strain and is introduced by epitaxial growth of Si and SiGe layers where the lattice mismatch between Si and SiGe causes a tensile strain. The increase of the electron mobility in channels of MOSFETs prepared on such substrates was extensively studied [31–33]. Furthermore, a variety of new substrates such as the strained Si/relaxed SiGe layers are formed on buried oxides (SiGe on insulator (SGOI)) and the strained silicon on insulator (SSOI), where strained silicon layers are directly bonded to buried oxides, have been demonstrated. The latter combines the advantages of SOI and biaxially strained silicon layers in a single substrate. In order to combine the different mobilities of electrons and holes, hybride-oriented substrates (HOTs) were introduced by IBM [34].

Uniaxial strain is generated by local structural elements near the channel region. Since these process modules that cause uniaxial strain are part of high-performance CMOS processes, uniaxial strain is also referred to as process-induced strain (PIS). The application of PIS does not require specific substrates. It can be applied on bulk wafers or SOI substrates. Owing to the relative ease of integrating process-induced strain modules in conventional CMOS processes, strain-enhanced scaling has relied on the development of new advanced methods of PIS. The application of local strain

elements, however, is limited by further scaling making some of them ineffective or unfeasible.

6.3.2 Local Strain

Electron and hole mobilities respond to mechanical stresses in different ways. For MOSFETs with the [110] channel orientation on (001)-oriented silicon substrates, tensile strain along the [110] direction improves electron mobility but degrades hole mobility. Therefore, to improve both the electron mobility in n-channel MOSFETs and the hole mobility in p-channel MOSFETs, different approaches for strain inducement in the p- and n-channel transistors are needed. Incorporating local strain to enhance MOSFET performance was first introduced by Ito *et al.* [35] and Shimizu *et al.* [36], who used etch-stop nitride, and by Gannavaram *et al.* [37], who used SiGe source/drain regions. Advanced CMOS processes include different process-induced stressors. These are mainly stressed contact layers, embedded source/drain stressors, stress memorization techniques, and stressed contact and metal gates (Figure 6.1).

Contact layers are typically stressed nitride layers deposited after salicidation on the top of devices. Tensile contact layers are deposited on nMOSFET and compressive contact layers are deposited on pMOSFET. The strain in the channel region depends on the intrinsic stress of the layer, thickness of the layer, and device dimensions. Using tensile and compressive contact layers (dual stress liner (DSL)), a significant hole and electron mobility enhancement was achieved [38]. Furthermore, important parameters of SOI CMOS devices, such as effective drive current enhancement, were proved in different 45 nm technologies.

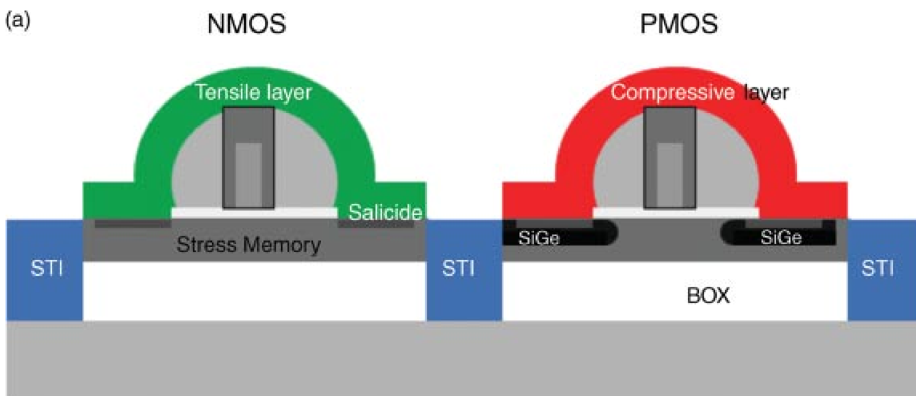

Figure 6.1 Schematic representation of local stressors (process-induced stressors) in SOI CMOS (a). Tensile strain in nMOSFET is obtained by tensile contact layers and various stress memorization techniques. Compressive strain in pMOSFET is induced by compressive contact layers and embedded SiGe. XTEM of SSOI nMOSFET without process-induced stressors (b), and SSOI pMOSFET with embedded SiGe and compressive overlayer (c).

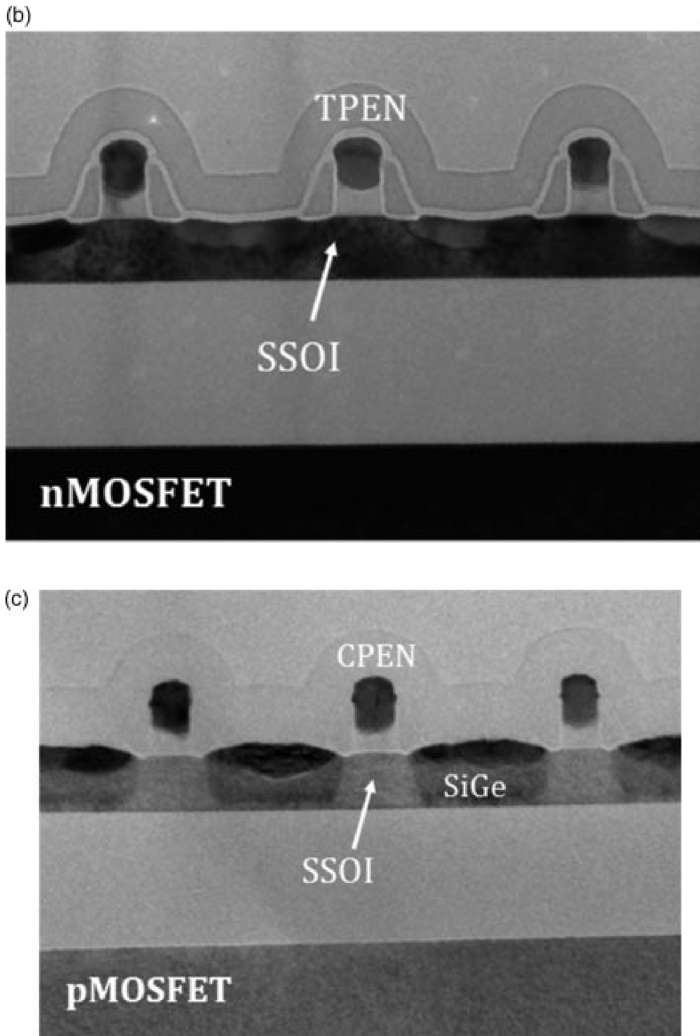

Figure 6.1 (*Continued*)

Stress memorization techniques (SMT) typically involve a preamorphization, a nitride capping layer, and an additional annealing process. SMT increases the nMOSFET drive current and degrade the pMOSFET device performance.

Embedded SiGe layers (eSiGe) deposited by epitaxial growth of SiGe alloys in cavities etched into the source/drain areas are used in pMOSFET transistors. Due to the larger lattice constant of SiGe compared to silicon, a compressive strain is induced in the channel of the pMOSFETs. This technique can be optimized and improved by combining SiGe and SiC layers for CMOS devices [39].

The impact of the increase of the carrier mobility in the channel of MOSFETs is an increase of the drain current. The correlation between the drain current (I_D) and the effective carrier mobility (μ_{eff}) is given in the linear region of the drain current–source/drain voltage (I_D–V_{DS}) characteristics of a MOSFET by the relation

$$I_D = \frac{W}{L}\mu_{eff} C_{ox}(V_{GS} - V_T) V_{DS} \tag{6.7}$$

where W and L are the channel width and length, respectively, V_{GS} is the gate/source voltage, V_T is the threshold voltage, and C_{ox} is the capacitance of the gate oxide. Measurements of the strain-induced mobility change $\Delta\mu$ and the corresponding change in linear drain current, however, show clear differences for n- and pMOSFETs [40]. A change of 50% in mobility results only in an increase of the drain current by 20%. In contrast, for pMOSFETs, a 40% increase in the drain current is obtained for the same change in mobility. The differences may be caused by the reduced source–drain resistance by the embedded SiGe channel in pMOSFETs originated from the lower SiGe valence band offset.

Different scattering mechanisms reduce the effect of strain on the mobility enhancement even in short-channel devices [41]. Here, the carrier mobility is expressed by an effective mobility μ_{eff} that is related to the carrier velocity v in the presence of low lateral fields E_{lat} by the equation

$$v = E_{lat} \cdot \mu_{eff} \tag{6.8}$$

In short-channel devices, carriers do not reach v_{sat} instantaneously; instead, in saturation regime, the carrier transport is more and more governed by ballistic transport [42]. Nevertheless, μ_{eff} at low lateral fields and v are correlated in scaled MOSFETs, although there is no general agreement about this correlation [43]. According to Lundstrom [44], the change in the saturation drive current $\Delta I_{D,sat}$ is

$$\Delta I_{D,sat} = \Delta\mu(1 - B) \tag{6.9}$$

where B is the ballistic efficiency and the saturation drive current $I_{D,sat}$ in the ballistic regime is given by [45]

$$I_{d,sat} = W v_T C_{ox}(V_{GS} - V_T) \tag{6.10}$$

where $C_{ox}(V_{GS} - V_T)$ is the charge density and

$$v_T = \sqrt{\frac{2k_B T_L}{\pi m_t^*}} \tag{6.11}$$

is the unidirectional thermal velocity [46] that depends on the strain-induced effective mass m_t^*. In Eq. (6.1), k_B is the Boltzmann constant and T_L is the temperature. Figure 6.2 shows the dependence of $\Delta I_{D,sat}$ on the change in mobility $\Delta\mu$. It can be seen that all data measured for n- and pMOSFETs are on a single curve with a similar slope for all strain techniques. The extracted value for B is about 0.61 for nMOSFETs and about 0.63 for pMOSFETs. From Eq. (6.9), it follows that an improvement of 50% in mobility causes an enhancement of the saturation current $I_{D,sat}$ by about 20% for n- and pMOSFETs.

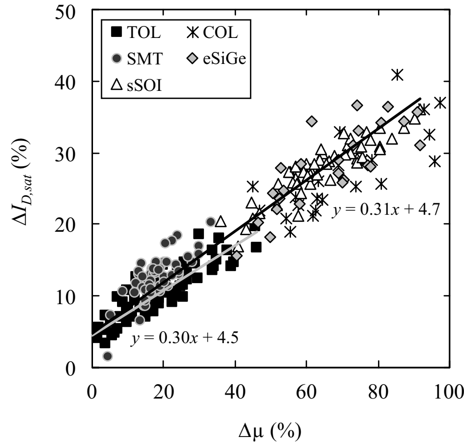

Figure 6.2 Correlation between carrier mobility change $\Delta\mu$ and the change in saturation drain current $\Delta I_{D,sat}$ for different local strain techniques for n- and pMOSFETs. TOL: tensile overlayer; COL: compressive overlayer; SMT: stress memorization technique; eSiGe: embedded SiGe channel; SSOI: strained silicon on insulator.

6.3.3
Global Strain

Global strain on wafer level is induced by the epitaxial growth of a Si layer on a $Si_{1-x}Ge_x$ buffer. Because the lattice constant of $Si_{1-x}Ge_x$ ($0 \leq x \leq 1$) alloys varies between 0.5431 nm for silicon ($x = 0$) and 0.5657 nm for germanium ($x = 1$), tensile strain is induced in the silicon layer epitaxially grown on top of the SiGe. The strain is generally biaxial. Furthermore, uniaxially strained layers can also be obtained by mechanical straining.

6.3.3.1 **Biaxially Strained Layers**

Various heterostructure substrates have been applied to realize biaxial strain and high-mobility channel materials [47]. Figure 6.3 illustrates various heterostructure substrates that have been employed to biaxial strain and high-mobility channel materials. Epitaxially grown $Si_{1-x}Ge_x$ layers on Si bulk wafers are generally applied acting as substrate for a strained silicon layer grown on top (bulk materials). In order to reduce the defect density in the strained silicon, a relaxed $Si_{1-x}Ge_x$ buffer is required grown on a graded $Si_{1-x}Ge_x$ layer (Figure 6.3a). Because the Ge concentration x increases continuously by about 10% per micrometer, the thickness of the graded buffer is several micrometers. An alternative is the relaxation of a thin pseudomorphic SiGe layer (<500 nm) induced by hydrogen or helium implantation and subsequent annealing [48]. A thinner SiGe buffer makes the process cost-effective. Variations of the basic structure have also been published, including dual channel structures incorporating an additional strained $Si_{1-y}Ge_y$ layer with $y > x$ (Figure 6.3b) and heterostructures on bulk using a second strained silicon layer

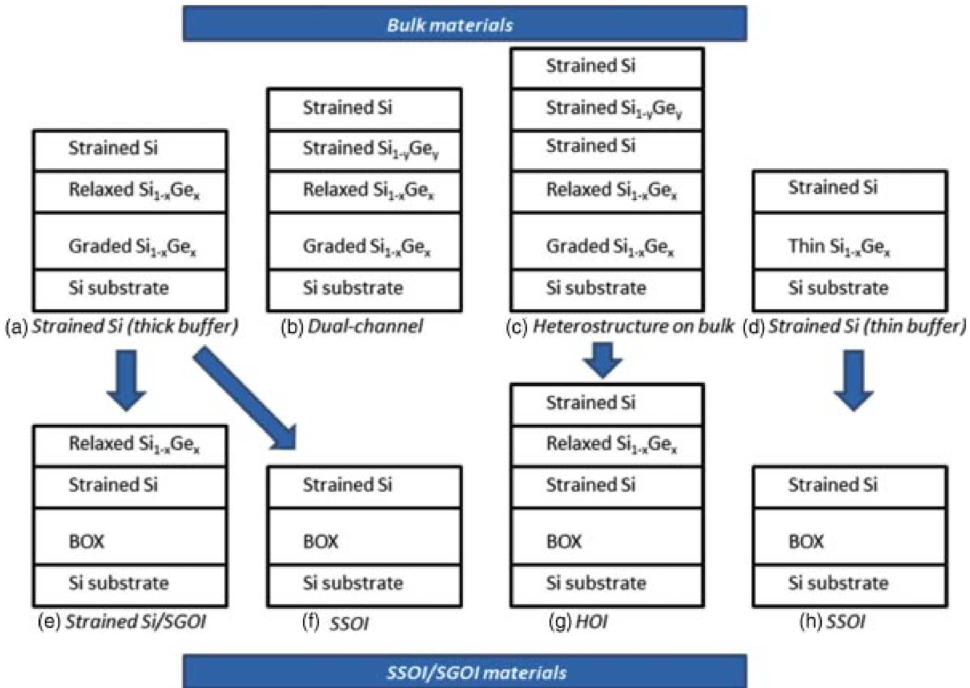

Figure 6.3 Schematic illustration of various heterostructure substrates produced by epitaxial growth on bulk substrates (bulk materials) and by transfer of the strained layers to oxidized substrates (strained silicon on insulator (SSOI), strained Si/SiGe on insulator (SGOI)) [46, 48].

(Figure 6.3c) [49]. Layer stacks of the different types have been applied as virtual substrates for the preparation of SSOI and SGOI wafers.

The realization of SSOI wafers from bulk materials is a complex process combining wafer bonding, layer transfer, and etch-back methods. The SSOI technologies provide a pathway to implementing mobility enhancement in partially or fully depleted devices, in ultrathin-body (UTB) MOSFETs, or nonplanar (double-gate) MOSFETs. Mobility enhancement in SSOI was reported in Refs [50, 51] for the different SSOI configurations. Furthermore, long-channel devices ($L_g \geq 1\,\mu m$) show clearly improvements of the device characteristics. For instance, drive current ($I_{D,sat}$) improvements of 80% at the same gate-to-drain leakage (I_{off}) have been measured. Improvements on the same order of magnitude were obtained only for short-channel devices if modified CMOS processes were applied in order to avoid interaction with process-induced stressors reducing the effect of the biaxial strain [18]. An electron mobility enhancement of about 40% and significant improvements of the I_{on}–I_{off} characteristics were obtained for nMOSFETs prepared in a 45 nm technology node on standard SSOI material (prepared on $Si_{0.78}Ge_{0.22}$ virtual substrates), which increases to about 60% if highly strained silicon layers are used (prepared on $Si_{0.69}Ge_{0.29}$ virtual substrates) [52]. Devices were prepared for these investigations

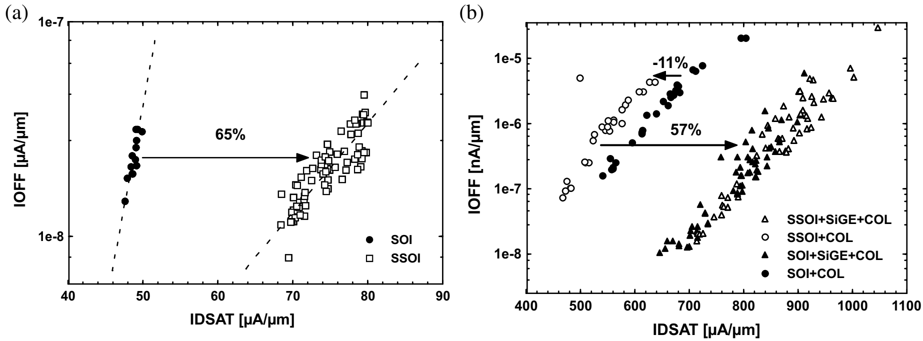

Figure 6.4 I_{off} versus $I_{D,sat}$ curves for n- and pMOSFETs prepared on SSOI and SOI substrates. The biaxial strain (SSOI) was combined with local stressors for pMOSFETs (SiGe: embedded SiGe channel; COL: compressive layer). An increase of $I_{D,sat}$ of 65% was obtained for long-channel ($W = L = 4.5$ µm) nMOSFETs (a), while the effect of different overlayers on short-channel ($L = 45$ nm) pMOSFETS is shown in (b).

using a fully depleted SOI (FDSOI) technology with a TiN/HfO_2 gate stack. The thickness of the Si device layer was 9 nm. It was demonstrated that the mobility enhancement also depends on the channel orientation. A mobility enhancement of 135% was found for nMOSFETs on highly strained silicon having ⟨110⟩-oriented channels. In addition, the hole mobility enhances in the same time for pMOSFETs with channel orientations parallel to ⟨100⟩. The analyses have also shown that a sufficient amount of strain is preserved in MOSFETs fabricated in technology nodes below 45 nm. A mobility enhancement for nMOSFETs up to 40% is attainable in a 15 nm technology [51].

This means that applications of SSOI wafers require modifications of existing CMOS processes. The combination of biaxially strained SSOI and optimized uniaxial stressors (dual-stress nitride capping layer and embedded SiGe) was demonstrated resulting in $I_{D,sat}$ improvements of 27% and 36% for n-channel MOSFETs and p-channel MOSFETs, respectively, in sub-40 nm devices [53]. In addition, the gate leakage current was also reduced by 30%. Figure 6.4 shows that a further adjustment of the CMOS process results in additional improvements. An increase of $I_{D,sat}$ of 65% was obtained for nMOSFETS. For pMOSFETs, the strain of the SSOI substrate is tensile in both the longitudinal (with current) and perpendicular directions. The longitudinal component degrades hole mobility, while the perpendicular strain enhances hole mobility. The net result is a decrease in hole mobility. This is shown in Figure 6.4b, where the longitudinal tensile strain counteracts the compressive overlayer, causing a 11% degradation in pMOSFET drive current. However, the addition of a cavity etch for embedded SiGe effectively relaxes this longitudinal tensile strain and allows pMOSFET performance to be in line with standard SOI. All investigations suggest that the combination of biaxially strained SSOI and uniaxial strain by process-induced stressors is the optimum way for future requirements [50, 52].

6.3.3.2 Uniaxially Strained Layers

A concept to realize uniaxial, tensile strain on wafer level was first published by Belford [54]. An approach of uniaxial compressive strain on wafer level based on wafer direct bonding of prestressed wafers was also published [55]. Two wafers were bent over a cylinder, thereby creating a curved or bowed wafer with a strained state induced. The bending direction was parallel to [110]. The curved wafers are brought into contact via direct wafer bonding and the covalent bonds across the bonded interface form upon annealing in the bent state. By combining the process with hydrogen-induced layer splitting, thin strained layers were transferred. The process can generally be used to realize strained layers of either tensile or compressive strain. The strain introduced by this technique is significantly lower as for biaxially strained layers. Depending on the radius of curvature, strain values between about 0.08% and 0.04% were obtained for a radius of curvature ranging from 0.5 to 1 m.

The concept of uniaxial strain on wafer level was originally applied to show the different behavior of uniaxial and biaxial strains on MOSFET performance [56].

6.4 Strain Engineering for 22 nm CMOS Technologies and Below

Numerous experiments over the past years proved the applicability of biaxially strained silicon, uniaxially strained silicon, and local strain elements, or combination of these in state-of-the-art device processes. A strained Si on SGOI substrate, for instance, was used to realize n- and p-MOSFETs with channel lengths up to 25 nm [57]. Mobility enhancements of 50% for electrons (with 15% Ge) and 15–20% for holes (with 20–25% Ge) have been demonstrated. Other investigations refer to a mobility enhancement of 46% for electrons and 60–80% for holes using SGOI with the same Ge concentration. An alternative process to attain SiGe layers with higher Ge content, that is, higher strain in the upper strained silicon layer, is the Ge condensation method [58]. The process consists of epitaxial growth of a strained SiGe layer with a low Ge fraction on a SOI substrate and successive high-temperature oxidation. SiGe layers having Ge fractions of more than 0.5 and large strain values over 1% were realized. A hole mobility enhancement by a factor of 10 was measured. Recently, however, variations of the threshold voltage are obtained on SGOI-MOSFETs fabricated by the Ge condensation process. It was verified that the variation of the threshold voltage can be attributed to the variation of strain in the Si channel layers. This variation was found to be correlated with the variation of the lattice spacing in the SGOI layer, which is caused by the nonuniform lattice relaxation in the SGOI layers during the condensation process [59].

Therefore, strained silicon on insulator without a buried SiGe layer appears to be more favorable. This is also true with respect to the process integration. Associated with the presence of the SiGe layer below the channel, issues such as Ge segregation at the Si/SiO_2 interface, enhanced As or P diffusion, limited thermal budget, and rapid dopant diffusion along misfit dislocations would be largely eliminated [49]. Most of the measurements reported until now show enhanced mobility data and

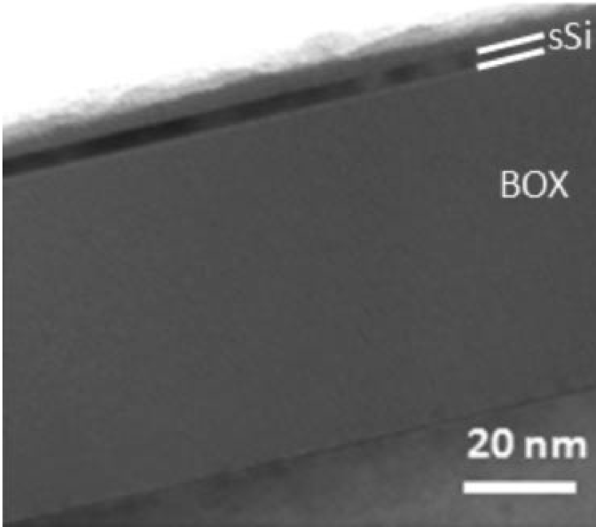

Figure 6.5 TEM cross-section image of a SSOI wafer. The thickness of the strained silicon (sSi) layer is 6.5 nm.

drive current improvements for both long- and short-channel devices having gate lengths of 60 nm and below. The sustainment of enhanced mobility and improved I_{on}/I_{off} characteristics for short-channel devices is mainly achieved by modifications of the CMOS process [50]. Process integration of SSOI materials in CMOS technologies is, therefore, an important issue [60].

The advantage of SSOI is the scalability to thinner device and insulator (BOX) layers, respectively. This allows the combination of strain with benefits of ultrathin-body MOSFETs [61]. Figure 6.5 shows the transmission electron microscope (TEM) image (cross-section image) of a SSOI wafer. The thickness of the strained silicon layer transferred by wafer bonding is only 6.5 nm. UTB SOI is an attractive option for device scaling, because it can effectively reduce the short-channel effect and eliminate most of the leakage paths. The ultrathin SOI thickness requirement for short-channel effect control in single-gate FETs can be relaxed by using a more complex double-gate FET that offers improved electrostatic gate control of the body. Numerical simulations indicate that scalability of double-gate FETs improves by a factor of 2.5–3 [62].

The reduction of the thickness of the silicon layer required for UTB MOSFETs also contributes to the strain conservation in the silicon layer. Figure 6.6a shows the dependence of the in-plane stress on the size (channel length) of devices for different thicknesses of the strained silicon layer (height in Figure 6.6a). It can clearly be seen that strain (or stress) relaxation is a function of the silicon layer thickness. Decreasing the layer thickness conserves the strain even for small structure sizes. This means that with the strained silicon layer at thickness below 10 nm (required for UTB SSOI MOSFETs) and gate length in the subnanometer range, the whole tensile strain is preserved. Varying the ratio of the structure length L to the thickness of the

layer (height H) causes different stress distributions in the structures (Figure 6.6b). While at $H/L = 1$, a sufficient (tensile) stress is located only at the Si/SiO_2 interface, the stress is preserved in the whole layer at $H/L = 0.13$. Furthermore, a compressive stress is obtained close to the surface at $H/L = 0.45$. This means that under specific conditions, devices with different stress behavior (tensile or compressive) within one device may simultaneously exist by applying biaxially strained SSOI wafers. The results of the simulation were experimentally verified by Raman measurements [63]. In addition, Raman and TEM analyses also proved the transformation of the biaxial strain into uniaxial strain by increasing the ratio of the width to the length of the structures. Figure 6.7 shows the results of finite element (FEM) simulations of the strain distribution in channels with different width/length (W/L) ratios. The thickness of the strained silicon layer was 20 nm and W/L was varied between 1 and 20 at a constant width of 50 nm. The initial biaxial strain in the unpatterned layer was $\varepsilon \cong 0.6\%$. At a square-like channel geometry ($W/L = 1$), the strain is more or less relaxed. A detectable strain of $\varepsilon \cong 0.3\%$ exists only at the bottom of the structure, that is, close to the interface to the buried oxide. Most of the initial strain is preserved in the longitudinal direction by increasing W/L. At $W/L = 10$, the initial strain value of $\varepsilon \cong 0.6\%$ is obtained for about two-thirds of half of the longitudinal direction and is

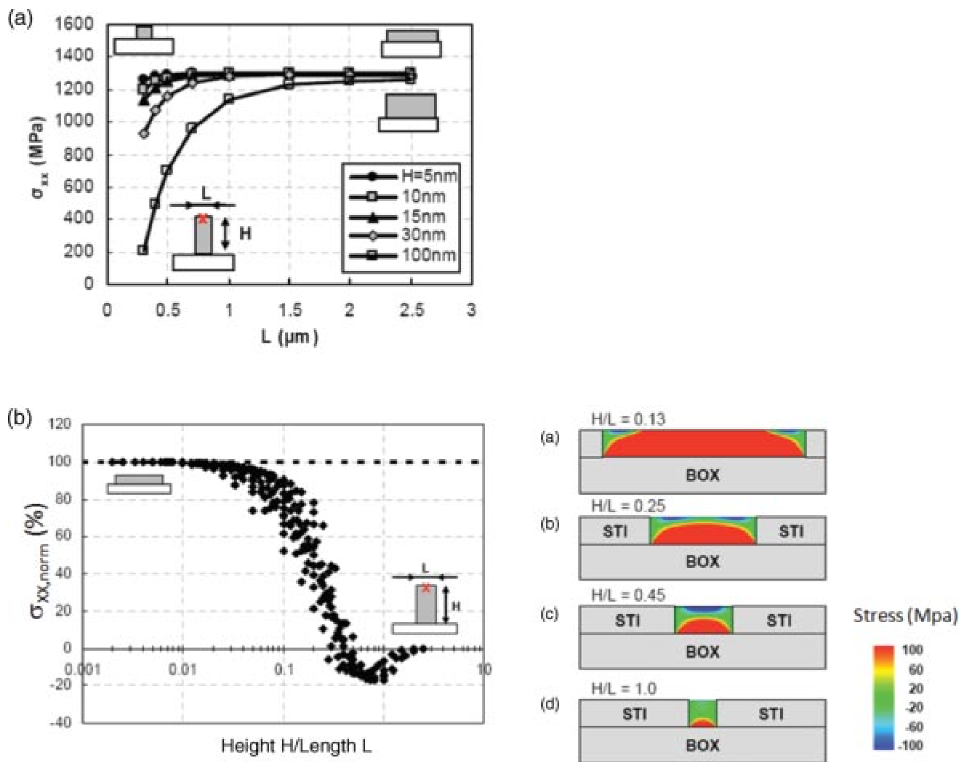

Figure 6.6 (a) Results of FEM simulations of the in-plane stress (σ_{xx}) as a function of the gate length L (a). The height H (or thickness) of the strained silicon layer was in the range of 5–100 nm. (b) Dependence of the in-plane stress on the height/length ratio of individual structures.

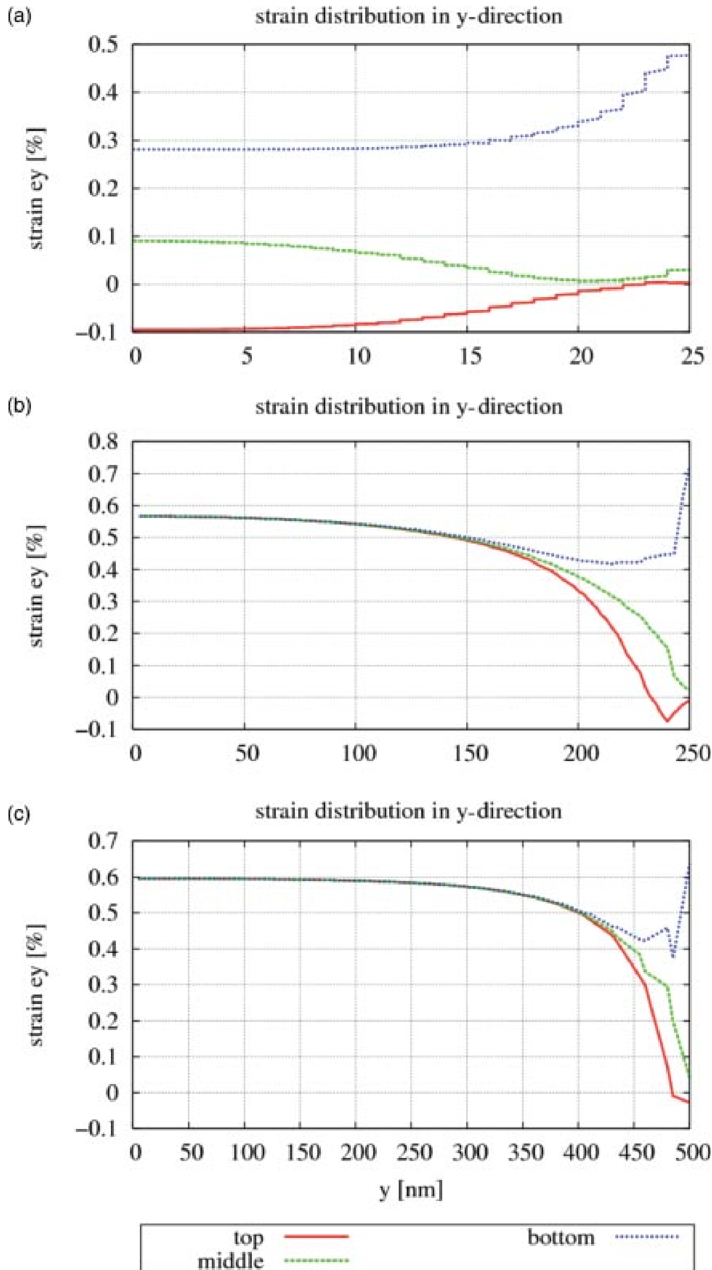

Figure 6.7 Remaining strain in the longitudinal direction of strained silicon channels (SSOI) having W/L ratios of 1 (a), 10 (b), and 20 (c). The strain was calculated at the top, middle, and bottom of the layer. Constant values of the channel width $W = 50$ nm and silicon layer thickness of 20 nm are used. FEM simulations of half of the channel length.

relaxed in the perpendicular direction. A more homogeneous strain profile and a lower strain relaxation at the end are found for $W/L = 20$. Because the strain is preserved in the longitudinal direction and relaxed in the orthogonal direction, the initial biaxial strain is altered to uniaxial strain. Therefore, biaxially strained layers, especially SSOI, are promising candidates to introduce strain in Si channels of sub-30 nm MOSFETS, where conventional local strain techniques cannot be applied.

6.5 Conclusions

Strained silicon channels are one of the most important *technology boosters* for further Si CMOS developments. The mobility enhancement obtained by applying appropriate strain provides higher carrier velocity in MOS channels, resulting in higher drive current under a fixed supply voltage and gate oxide thickness. Process-induced stressors including tensile or compressive contact layers and various stress memorization techniques are already integrated in today's high-performance technologies. The application of local strain elements, however, is limited by further scaling. On the other hand, one of the most important advantages of globally strained SSOI is the scalability to thinner device and insulator layers. This allows the combination of strain with benefits of ultra-thin-body MOSFETs. The reduction of the thickness of the silicon layer contributes to the strain conservation. Furthermore, varying the relation between channel length and layer thickness can introduce both types of strain and the modification of the biaxial into uniaxial strain.

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