# 5

# THE OPERATIONAL AMPLIFIER AS A CIRCUIT ELEMENT

## 5.1 INTRODUCTION TO THE OPERATIONAL AMPLIFIER

The operational amplifier, more commonly known as *op amp,* is an analog circuit. Op amps perform many arithmetic functions, linear and nonlinear operations in the analog or continuous domain. Op amps are also used in several kinds of analog amplifiers and active filters. They are also used to implement nonlinear circuits such as voltage comparators and continue to have a widespread use in the field of analog electronics. In its very early years of electronics, the beginning of the twentieth century, the first op amps were implemented with vacuum tubes, later on with transistors, and most currently, op amps are available in a single (or monolithic) integrated circuit (IC) device. That is to say that the transistors that implement the op amp itself reside within the IC. Why, if the basic components of an op amp are transistors, do we choose to cover op amps prior to the introductory chapter on electronic devices (*diodes, bipolar*, and *MOSFET transistors*)? The reason is simple and justifiable: op amps can be dealt with as circuit elements without necessarily knowing all the details of their internals. In this chapter we will start using dependent sources, to model the operation of op amps. Moreover, the op amp can perform a variety of functions that can be easily understood without initially having the knowledge of how the actual integrated circuit is designed. Finally, an op amp can be effectively used as a circuit element knowing the behavior of its

inputs and output terminals and knowing its parameters from the manufacturer's data sheet. Op amp parameters are indicators of how much a real op amp deviates from an idealized model of an op amp. It is in the interest of the circuit designer using op amps to establish when the op amp-based circuit behaves as if its op amps were ideal and when they are not. When op amp-based circuits have nonidealities, the circuit designer has to take such deviations from the ideal op amp into account to predict their circuit behavior more accurately.

## 5.2   IDEAL AND REAL OP AMPS

It is extremely useful to use a model of an idealized op amp. In many applications, as we will see later throughout this chapter, the idealized behavior is just a first-order approximation of the way the op amp works as a circuit element. Later on, we will add the influence of the real op amp parameters that may not let an op amp-based circuit to always be analyzed as an idealization. Our goal in this chapter is to understand the ideal op amp, understand how its inputs and output work. It is also our goal to know when and what to take into account from the manufacturer's data sheet, which otherwise would not be correct with the idealized model. Finally, one of our goals is to address and analyze the most important and useful linear and nonlinear applications using op amps.

The most basic symbol of an op amp is given in Figure 5.1. It has two inputs, a noninverting or positive input and an inverting or negative input. It also has a single output. The most generic way of representing an op amp, whether it is a real one or an idealized one, is the one seen in Figure 5.1a. A more complete graphical representation is to draw the power terminals that provide positive and negative power sources to the real op amp internals, Figure 5.1b. *Warning* to the reader: some technical publications, data sheets, or textbooks draw the positive input at the top left of the op amp symbol, some others draw the negative input at the top left. However, many other publications interchange the location of the positive and negative inputs. Thus, the reader has to be very cautious and find out which are the noninverting and the inverting inputs of the op amp. Confusing the correct input may mislead one into a completely incorrect interpretation of the function of an op amp-based circuit.

Some of the most basic ideal op amp characteristics are

(a)  Open-loop gain is infinite: $\infty$, or $A_{OL} \to \infty$

(b)  The noninverting and inverting terminals do not draw or source any current from or into the op amp. $Z_{input} = Z_i = \infty$, means that its input impedance is infinitely high.

(c)  The output of the op amp can provide an infinitely large current. In other words, the op amp output impedance is zero ($Z_{output} = 0$ or $Z_o = 0$).
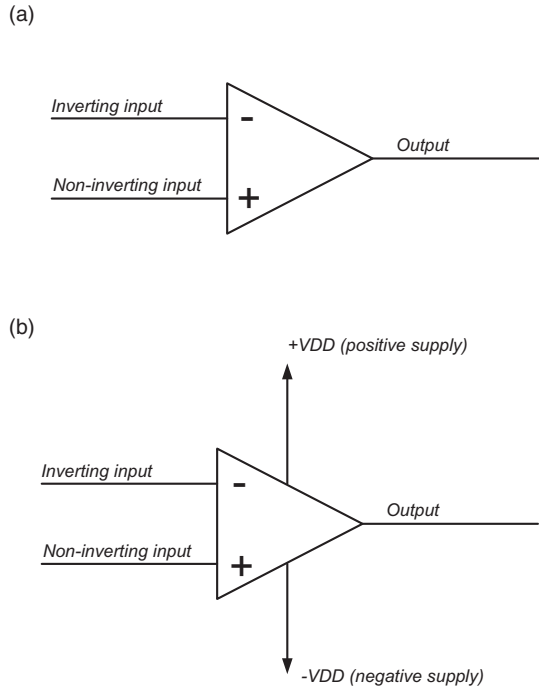
(a)



(b)



**Figure 5.1**   Graphic representation of an op amp (a) idealized or real op amp without power terminals, (b) real op amp showing its power terminals.

(d) When the op amp is operated in linear mode using negative feedback, the voltage difference between the noninverting and inverting input is infinitesimally small.

$$\Delta V = V^+ - V^- \to 0$$

We will come back to the negative feedback concept shortly.

(e) Bandwidth of an ideal amplifier is infinite, because the ideal amplifier can react to signals of any frequency equally well. Bandwidth in a real op amp refers to small signal bandwidth, that is, signals whose peak-to-peak amplitudes are a small fraction of the op amp power supply rail. For example, signals of a 1 V for a ±15-V powered op amp are considered to be small signal amplitudes.

(f) Slew-rate: For large signal behavior, that is, for signals that are comparable to the power supply rail magnitude in a real op amp, slew-rate is a finite and nonzero number. This is because real op amps take time to react to large voltage swings. Typically, slew-rates are expressed in volts per microsecond.

**Table 5.1   Some operational amplifiers idealizations**

| Parameter | Ideal Value |
| --- | --- |
| Open-loop gain ($A_{OL}$) | Infinite |
| Input resistance $R_i$ (more generically input impedance) | Infinite |
| Output resistance $R_o$ (more generically output impedance) | Zero |
| Voltage difference ($\Delta V$) between noninverting and inverting inputs, when negative feedback path exists. That is, the op amp is working in a linear application. **Note:** This is not true when the op amp operates in open-loop mode or with positive feedback. | Zero |
| Bandwidth (refers to small signal response capability) | Infinite |
| Slew-rate (refers to large signal response capability) | Infinite |
| Offset voltage | Zero |
| Bias current | Zero |
| Offset current | Zero |
| Common Mode Rejection Ratio (CMMR) | Infinite |

(g)   Offset voltage: Zero for the ideal case. This value is nonzero for real op amps since their negative and positive inputs cannot be perfectly matched.

(h)   Bias current: Zero for an ideal op amp. This value is nonzero for real op amps since their negative and positive inputs cannot be perfectly matched.

(i)   Offset current (difference of bias currents at positive and negative inputs): Zero for the ideal op amp. This value is nonzero for real op amp because bias currents, even when finite, cannot be perfectly matched.

(j)   Common Mode Rejection Ratio (CMRR): The ratio of differential mode gain and the common mode gain, usually expressed in dBs.

Table 5.1 summarizes the idealizations made above for an ideal op amp.

As we discuss more op amp-based circuits, we will introduce some more of the ideal op amp characteristics. We will be able to go a long way using the top four characteristics mentioned in Table 5.1. For now, in what way real op amps parameters differ from the idealizations of Table 5.1? Without getting into much detail this early in the chapter, we will just say that for a real op amp, none of the characteristics listed in Table 5.1 is true. Upon studying real op amp data sheet parameters, we will expand what that means in a more qualitative manner.

## 5.3   BRIEF DEFINITION OF LINEAR AMPLIFIERS

Let us study the basic linear amplifiers that are available, before we zoom into the operational amplifier-based circuits. Op amp-based circuits are usually

special cases of the most generic cases of the four types of amplifiers that we will cover in this section.

An amplifier is a two-port device that receives an input signal and produces and output that is proportional to some constant, that we call the amplifier *gain* or *A,* which stands for amplification factor. In general, the *gain* of an amplifier (unlike the gain of an ideal op amp) is finite. Generally when we talk about amplifiers, we will always refer to linear amplifiers, unless it is otherwise stated. For example, multipliers are nonlinear amplifiers, whereas adders, sub-tractors, inverters, buffers, and difference amplifiers all are linear amplifiers.

Four key types of linear amplifiers exist from the point of view of the kind of input and output signals that they involve:

(a)  Voltage amplifier
(b)  Current amplifier
(c)  Trans-conductance amplifier
(d)  Trans-resistance amplifier

A voltage amplifier receives an input voltage and produces an amplified output voltage. A current amplifier receives an input current and produces an ampli-fied output current. A trans-resistance amplifier receives an input current and produces an amplified output voltage. A trans-conductance amplifier receives an input voltage and produces an amplified output current.

It is common practice to cascade amplifiers. That means connecting the output of one into the input of the next one. It is common to cascade two or three stages of amplifiers in that way. The input stage of an amplifier typically loads the output of an amplifier that precedes it. Figure 5.2 presents three cascaded amplifiers.

Figure 5.3 depicts the four amplifiers types described above.

The voltage amplifier of Figure 5.3a has an ideal infinite input resistance, a zero output resistance, and a voltage gain of

$$R_i \rightarrow \infty$$

$$R_o = 0$$

$$A_v = v_o / v_i. \tag{5.1}$$

The current amplifier of Figure 5.3b has an ideal zero input resistance, an infinite output resistance, and a current gain of
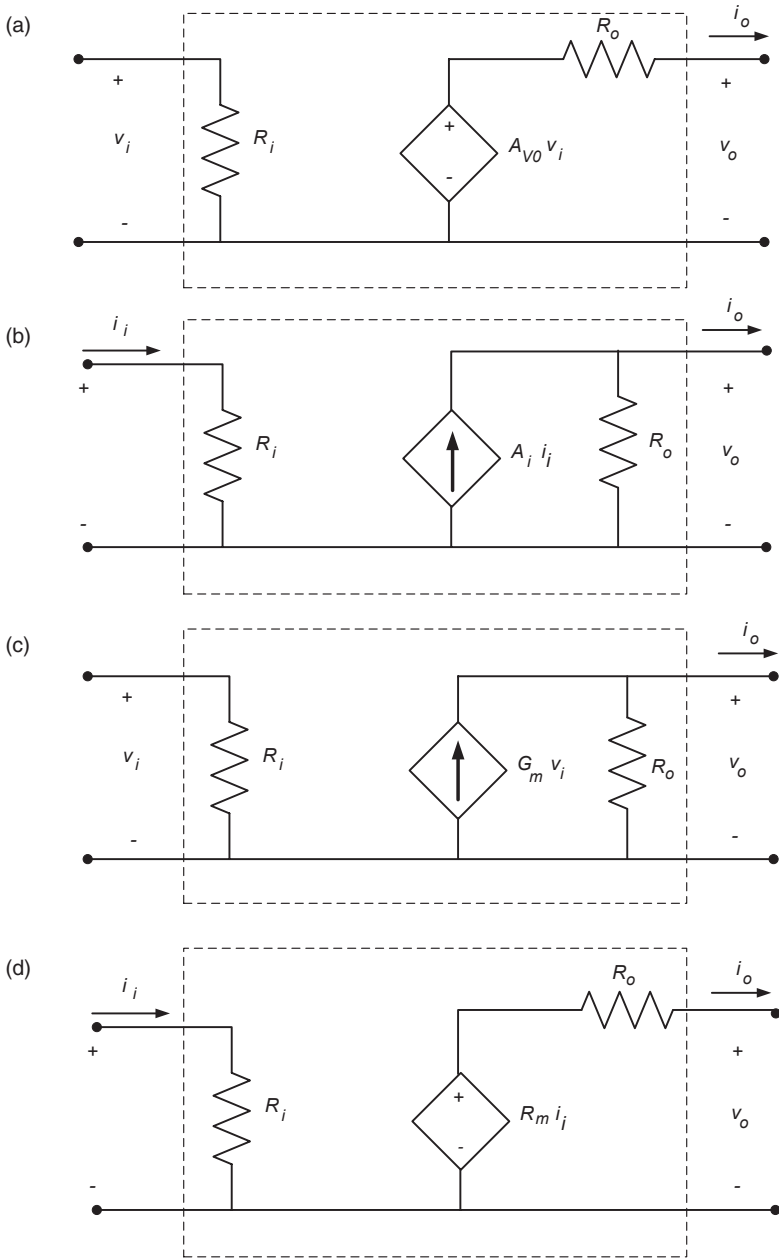


**Figure 5.2**  Cascaded amplifiers.

**Figure 5.3**   Amplifier types: (a) voltage, (b) current, (c) trans-conductance, (d) trans-resistance.

$$R_i = 0$$

$$R_o \to \infty$$

$$A_I = i_o / i_i. \tag{5.2}$$

The trans-conductance amplifier of Figure 5.3c has an ideal infinite input resistance, an infinite output resistance, and a trans-conductance gain of

$$R_i \to \infty$$

$$R_o \to \infty$$

$$A_G = i_o / v_i. \tag{5.3}$$

The trans-resistance amplifier of Figure 5.3d has an ideal zero input resistance, a zero output resistance, and an open circuit trans-resistance gain of

$$R_i = 0$$

$$R_o = 0$$

$$A_R = v_o / i_i. \tag{5.4}$$

But what do Equations (5.1) through (5.4) mean? Let us start with Equation (5.1) on the voltage amplifier and let us refer to Figure 5.3a. The voltage amplifier is modeled with a voltage-controlled voltage source (VCVS). A voltage amplifier has an input resistance (in more general terms we say that it is an input impedance), and from an ideal point of view, we do not want the input stage of the amplifier to load the source that is driving it. So that is the reason why, ideally speaking, a voltage amplifier should have an infinite input resistance. This in effect means that the amplifier does not draw any current from its driving source. A finite output resistance of a voltage amplifier is what would actually limit a real amplifier from driving current to a load connected across its output terminals. Since ideally one wants the amplifier to have no current sourcing limitation, thus we say that the ideal voltage amp should have a zero output resistance.

For the current amplifier of Figure 5.3b the amp is modeled by a current-controlled current source (CCCS). The controlling input is the input current $i_i$; we want the amplifier to be controlled by the current and not by a voltage developed across its input resistance. Thus, in this case, the ideal current amplifier should have a zero input resistance, since the input current has to enter the amplifier for control purposes. For the same amplifier, notice that the output resistance is in parallel with the output current source $A_i i_i$; we certainly do not want all the output current to be drained or consumed by its output resistance, we want the output current to go to the load. Thus, the output resistance of an ideal current amplifier wants to be infinite. The trans-conductance amplifier of Figure 5.3c is modeled with a voltage-controlled

current source (VCCS). The controlling input is voltage $v_i$, so we want the ideal trans-conductance amplifier not to draw any current from its driving input source; thus, the need for an infinite input resistance. The infinite output resistance of the trans-conductance amp is justified in the same way as the output resistance of the current amplifier was. The trans-resistance amp is modeled with a current-controlled voltage source (CCVS); the input is controlled by current $i_i$, thus we want a zero input resistance for the trans-resistance amplifier, just like we have it for the current amplifier. The output of the trans-resistance amplifier of Figure 5.3d behaves just like the output of the voltage amplifier, thus we want the ideal trans-resistance amplifier to have a zero output resistance to drive any load. Finally, let us note that the gain of the trans-resistance ($A_R$) and trans-conductance ($A_G$) amplifiers have respectively units of ohms and ohms$^{-1}$. Current and voltage amplifiers have dimensionless amplification factors.

## 5.4   LINEAR APPLICATIONS OF OP AMPS

Linear applications of op amps refer to those circuits that have a linear relationship between output and input, whereas nonlinear applications do not. The most common linear applications are inverting amplifiers, noninverting amplifiers, buffers, and difference amplifiers. Other interesting op amp-based linear circuits are integrators and differentiators.

### 5.4.1   The Inverting Amplifier

Let us now look at op amp-based circuit show of Figure 5.4. This circuit is called an inverting amplifier configuration. To analyze how this circuit works, we will assume that the op amp of the inverting amplifier is ideal. Let us carefully describe by inspection of Figure 5.4 how this circuit is connected. First,
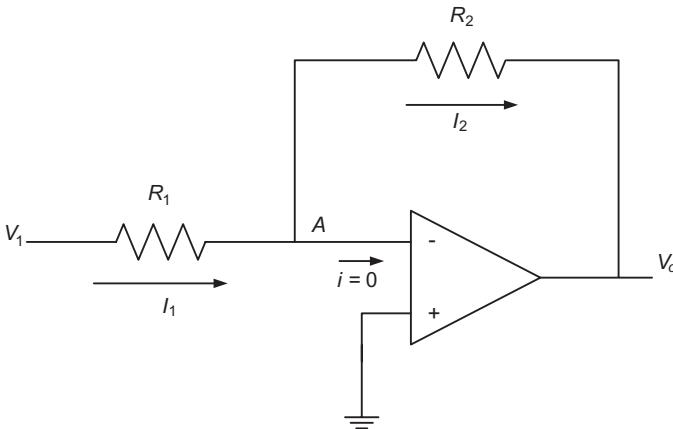


**Figure 5.4**   Op amp-based inverting amplifier configuration.

besides the op amp, we have two external resistors. Resistor $R_1$ is connected from the input source $V_1$ to the inverting input terminal of the op amp. Resistor $R_2$ connects the output of the op amp back to the inverting input of the op amp. This path from the output to the inverting input of the op amp is referred to as a negative feedback path. We will see that all linear circuits implemented with op amps have a negative feedback path. Finally, the noninverting input of the op amp is tied to reference ground.

**Example 5.1**  Calculate the output voltage to input voltage ratio, $V_o/V_i$ or the voltage gain of the circuit of Figure 5.4, assuming that the op amp is ideal.

Because the op amp has a negative feedback path, we can assume that the voltage difference between inverting and noninverting inputs is zero (see Table 5.1). Now because the noninverting input is tied to ground, then the voltage at the inverting input is referred to as being virtually grounded. People refer to as this node as being "virtual ground." The closer is the op amp to the idealization, the truer that statement becomes. Now we can state a Kirchoff's current law (KCL) equation at virtual ground node $A$:

$$I_1 = I_2 \tag{5.5}$$

because $i = 0$.

But since

$$I_1 = \frac{V_1}{R_1} \tag{5.6}$$

because node $A$ is virtually grounded, and since

$$I_2 = -\frac{V_A - V_o}{R_2} = -\frac{V_0}{R_2}, \tag{5.7}$$

$V_A$ is zero because it is *virtually grounded.*

At this point, let us refer to Figure 5.4 one more time. Note that the entire current $I_1$ that flows through $R_1$ also flows through $R_2$, because there is no current at all going into or out of the inverting terminal of the ideal op amp, $i = 0$, Equation (5.5).

So now combining Equations (5.6) and (5.7) yields:

$$\frac{V_o}{V_1} = -\frac{R_2}{R_1}. \tag{5.8}$$

Equation (5.8) is the approximated closed-loop voltage gain of the inverting amplifier, which assumes an infinite op amp $A_{OL}$. Equation (5.8) is also commonly referred to as the inverting amplifier closed-loop gain (CLG). Such

CLG is approximate because the ideal op amp parameters have been assumed (Table 5.1). Note that the absolute magnitude of this gain is the ratio of $R_2$ and $R_1$, whereas its sign is negative. It is important to observe that the CLG of the amplifier, Equation (5.8), depends only on the external resistors, and it is independent of the op amp, as long as the op amp open-loop gain is "large enough" and other op amp idealizations are met (Table 5.1).

### 5.4.1.1 Effects of Finite Op Amp Open-Loop Gain in the CLG  Now let us investigate what happens when the open-loop gain of the op amp is large, but not quite as large as it would have to be. We will see next how to quantify when the open-loop gain of the op amp is large enough for Equation (5.8) to be accurate. We will calculate the error we make using Equation (5.8) when the open-loop gain is finite. Figure 5.5 shows an op amp model where the open-loop gain is no longer infinite ($A_{OL} < \infty$). The output is modeled with a VCVS that depends on $\Delta V$, which is the difference between the noninverting and the inverting input voltages.

Upon making the above assumptions, not only $A_{OL}$ is finite but also $\Delta V$ is no longer zero. Figure 5.5 shows the usage of the model of a configured as an inverting amplifier with two external resistors, $R_1$ and $R_2$.

Let us assume that the one nonideality of the op amp model that we are interested in is its finite open-loop gain. By inspection of the circuit of Figure 5.5 we can state that

$$I_1 = I_2.$$

Because the op amp model still assumes that the input resistance of the op amp is infinite, thus
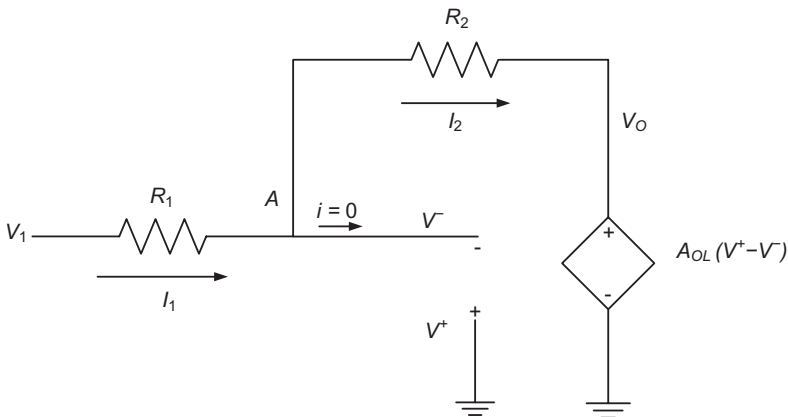
$$i = 0.$$



**Figure 5.5**  Modeling finite open-loop gain: model used to analyze an inverting configuration CLG with a finite-open-loop gain op amp.

Additionally,

$$(V_1 - V_A)/R_1 = (V_A - V_o)/R_2. \tag{5.9}$$

Since the open-loop gain is assumed to be finite, then

$$|V_A| = |V_o / A_{OL}|.$$

And since the positive input is grounded (0 V), the voltage at node $A$ has to be

$$V_A = -V_o / A_{OL}. \tag{5.10}$$

Using Equation (5.10) in Equation (5.9) and doing a little bit of algebra we arrive at

$$V_o / V_1 = -\frac{R_2 / R_1}{1 + \dfrac{1}{A_{OL}}(1 + R_2 / R_1)}. \tag{5.11}$$

Equation (5.11) shows the CLG of the inverting amplifier of Figure 5.4 when the open-loop gain is finite. We will also refer to this as the true value CLG. Note that if

$$A_{OL} \to \infty,$$

then Equation (5.11) becomes

$$V_o / V_1 = -R_2 / R_1. \tag{5.12}$$

Equation (5.12) is the CLG of the inverting amplifier with an infinite $A_{OL}$ op amp or simply the estimated or approximated CLG.

**Example 5.2**  Assume a ratio of $R_2/R_1 = 1$, using Equation (5.11), evaluate $V_o/V_1$ for the following values of $A_{OL}$: 1, 10, $10^2$, $10^3$, $10^4$, $10^5$, $10^6$, and $10^7$. Determine the error that exists between the more accurate close loop gain of Equation (5.11) with respect to the approximated CLG given by Equation (5.12).

Let us define the absolute value of the error between the two CLGs as the difference of the absolute values of Equations (5.12) and (5.11):

$$Abs\_Error = Estimated\_Value - True\_Value$$

$$Abs\_Error = \left| -R_2 / R_1 \right| - \left| -\frac{R_2 / R_1}{1 + \dfrac{1}{A_{OL}}(1 + R_2 / R_1)} \right| \qquad (5.13)$$

And the relative error:

$$Relative\_Error = (Abs\_Error / True\_Value) \times 100 \ [\%]$$

$$Relative\_Error = \left| \frac{\left( R_2 / R_1 - \dfrac{R_2 / R_1}{1 + \dfrac{1}{A_{OL}}(1 + R_2 / R_1)} \right)}{\dfrac{R_2 / R_1}{1 + \dfrac{1}{A_{OL}}(1 + R_2 / R_1)}} \right| \times 100. \qquad (5.14)$$

Table 5.2 depicts an inverting amplifier CLG absolute and relative errors for various finite values of $A_{OL}$ for a CLG of 1. Table 5.3 depicts the same values as Table 5.2 but for a CLG of 10.

It is interesting and important to note that for small CLG of 1 of an inverting amplifier, for a finite op amp open-loop gains ($A_{OL}$) of 60 dB and higher (Table 5.2), the relative error that exists between the CLG assuming an op amp with an infinite open-loop gain versus the CLG with a finite op amp open-loop gain is just 0.2%. This is quite a small error for the CLG equation. Since most op amps today have gains of at least 80 dB, the closed-loop error gain of the inverting amplifier with finite $A_{OL}$ is practically the same as the

**Table 5.2   Inverting amplifier closed-loop gain (CLG) errors for finite $A_{OL}$ and CLG of 1**

| Finite Op Amp Open-Loop Gain ($A_{OL}$) | Op Amp $A_{OL}$ in dB | Closed-Loop Gain of 1 (CLG = 1) with Finite $A_{OL}$ | CLG = 1 Absolute Error | CLG = 1 Relative Error |
|---|---|---|---|---|
| (V/V) | (dB) | (V/V) | (V/V) | (%) |
| 1 | 0 | 0.333333 | 0.666667 | 200.000000 |
| 10 | 20 | 0.833333 | 0.166667 | 20.000000 |
| 100 | 40 | 0.980392 | 0.019608 | 2.000000 |
| 1,000 | 60 | 0.998004 | 0.001996 | 0.200000 |
| 10,000 | 80 | 0.999800 | 0.000200 | 0.020000 |
| 100,000 | 100 | 0.999980 | 0.000020 | 0.002000 |
| 1,000,000 | 120 | 0.999998 | 0.000002 | 0.000200 |
| 10,000,000 | 140 | 1.000000 | 0.000000 | 0.000020 |

**Table 5.3   Inverting amplifier closed-loop gain (CLG) errors for finite $A_{OL}$ and CLG of 10**

| Finite Op Amp Open-Loop Gain ($A_{OL}$) | Op Amp $A_{OL}$ in dB | Closed-Loop Gain of 10 (CLG = 10) with Finite $A_{OL}$ | CLG = 10 Absolute Error | CLG = 10 Relative Error |
|---|---|---|---|---|
| (V/V) | (dB) | (V/V) | (V/V) | (%) |
| 1 | 0 | 0.833333 | 9.166667 | 1,100.000000 |
| 10 | 20 | 4.761905 | 5.238095 | 110.000000 |
| 100 | 40 | 9.009009 | 0.990991 | 11.000000 |
| 1,000 | 60 | 9.891197 | 0.108803 | 1.100000 |
| 10,000 | 80 | 9.989012 | 0.010988 | 0.110000 |
| 100,000 | 100 | 9.998900 | 0.001100 | 0.011000 |
| 1,000,000 | 120 | 9.999890 | 0.000110 | 0.001100 |
| 10,000,000 | 140 | 9.999989 | 0.000011 | 0.000110 |

gain with an infinite op amp open-loop gain (just a 0.02% error; again refer to Table 5.2). Now when the CLG of the inverting amplifier is higher than 1, in our example of Table 5.3, we assume a CLG of 10, note that for a finite open-loop gain of 60 dB, the CLG relative error of the amplifier is 1.1% (Table 5.3).

We can generalize and state that the larger the op amp $A_{OL}$, the more accurate is the approximated CLG of Equation (5.8). When the op amp $A_{OL}$ is not as large, then Equation (5.11) should used for better accuracy. However, once we have selected "an" op amp, $A_{OL}$ is fixed. So under these conditions, as presented by the Tables 5.2 and 5.3, the larger the CLG that is desired, the less accurate it will be when compared to another CLG that is smaller. For example, this is to say that given an op amp with a 100 dB $A_{OL}$, implementing an inverting configuration of a CLG of 1 will be more accurate than an inverting configuration of a CLG of 10. Once more looking at Tables 5.2 and 5.3, we have an error of 0.002% for a CLG of 1 and an error of 0.011% for a CLG of 10, in both cases for an $A_{OL}$ of 100 dB.

*5.4.1.1.1   Effect of Op Amp Output Swing Due to Saturation*   A real op amp has to receive power from positive and negative power supplies. Some op amps are designed to operate off a unipolar power supply; we will in general assume that the op amps we use require plus and minus power supplies unless it is otherwise stated. So we need to ask ourselves the following question, what can the maximum output of an op amp be? Regardless of whether the op amp is used in a linear or a nonlinear application, closed-loop or open-loop (will cover open-loop applications when talking about comparators), the highest and lowest output of the amplifier cannot exceed its power supply rails minus a saturation voltage ($V_{SAT}$) imposed by the op amp. For example, if an op amp is operated from a +15-V and −15-V power supplies, if the op amp

$V_{SAT}$ is 2 V *below the positive rail* and 2 V *above the negative rail*, its output shall always be within a voltage range of −13 V to +13 V. From now on, even though we will continue to deal with ideal op amps, we will assume that our ideal op amp requires positive and negative power, and its output shall be required to stay away from the saturation limits.

**Example 5.3**   Design an inverting amplifier with resistors and assume you have an ideal op amp. Let us assume that we want a CLG of −4. (a) Determine some possible resistor value pairs. (b) Determine the maximum and minimum input signal values not to saturate the op amp. Assume the op amp is powered from +15 V/−15 V supplies and for the output not to saturate the op amp is allowed excursions from +13 V to −13 V.

### *Solution to Example 5.3*

(a) the simplest combination of values that come to mind are 4 kΩ and 1 kΩ resistors. Other combinations of values such as 80 kΩ and 20 kΩ, or 400 kΩ and 100 kΩ are possible. This should pose a question on our mind: how large or how small such resistor values can be. Could we use a 400 MΩ and a 100 MΩ? Since we are assuming that we are dealing with an ideal op amp even 400 MΩ and 100 MΩ are fine to use because their ratio provides a CLG of −4 in an inverting amplifier configuration. *Later on we will see that it may not be possible to use arbitrarily large or arbitrarily small resistor values when we use real-world op amps. We will see that there are upper limits as well as lower limits for the resistor values we can choose.*

(b) Now, since the op amp output swing cannot exceed +13 V and cannot be under −13 V, the largest possible input signal magnitude is determined by dividing:

$$13 / 4 = 3.25 \text{ V}. \tag{5.15}$$

So the input signal should not exceed +3.25 V and should not be under −3.25 V for the inverting amplifier not to saturate. Why? Because if the input signal is +3.25 V, then

$$3.25 \text{ V}.(-4) = -13 \text{ V}, \tag{5.16}$$

and when the input signal is

$$-3.25 \text{ V}.(-4) = +13 \text{ V}. \tag{5.17}$$

So keeping the input within −3.25 V and +3.25 V voltage range will prevent the op amp from saturating. This is sometimes referred to as *the op amp hitting or exceeding the power rails.*

What happens, with the circuit of Example 5.3, when we saturate the op amp-based inverting amplifier? If the input is outside of the voltage range discussed, that is, ±3.25 V, the output of the op amp will not try to go beyond its positive output saturation voltage ($V_{SAT}$) or below its negative saturation voltage ($-V_{SAT}$). Figure 5.6a,b,c present three examples of what occurs when the inverting amplifier op amp output becomes saturated. In essence, the op amp-based circuit ceases to work as the inverting amplifier that we were trying



**(a)**

Input Signal

5 V — Inverting Amplifier Input signal : 5 V

0 V

time

Output Signal 15 V — Op amp positive supply rail

10 V

5 V

0 V

time

−5 V

−10 V

Inverting Amplifier output signal.
Actual Vo due to amplifier saturation = −13 V

−15 V ← Op amp negative supply rail
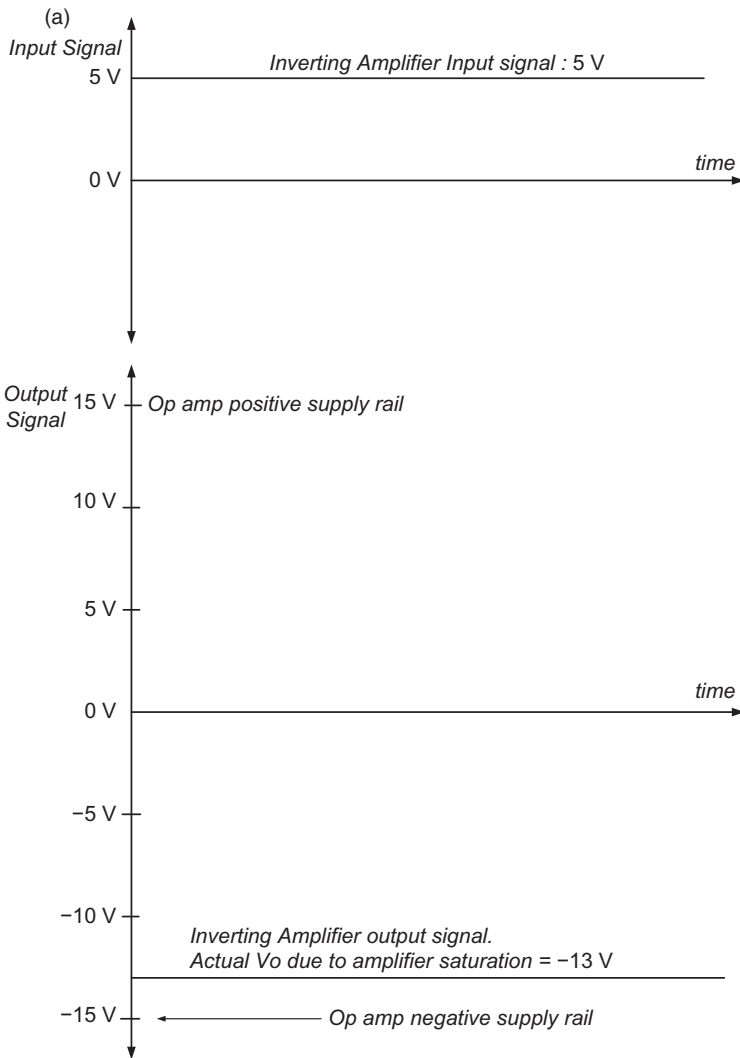
**Figure 5.6**   Inverting amplifier (*gain* = −4) circuit with signals exceeding the output saturation limits. (a) 5 V DC input, (b) −5 V DC input, and (c) 5 sin (2π 1 kHz) sinusoidal input.
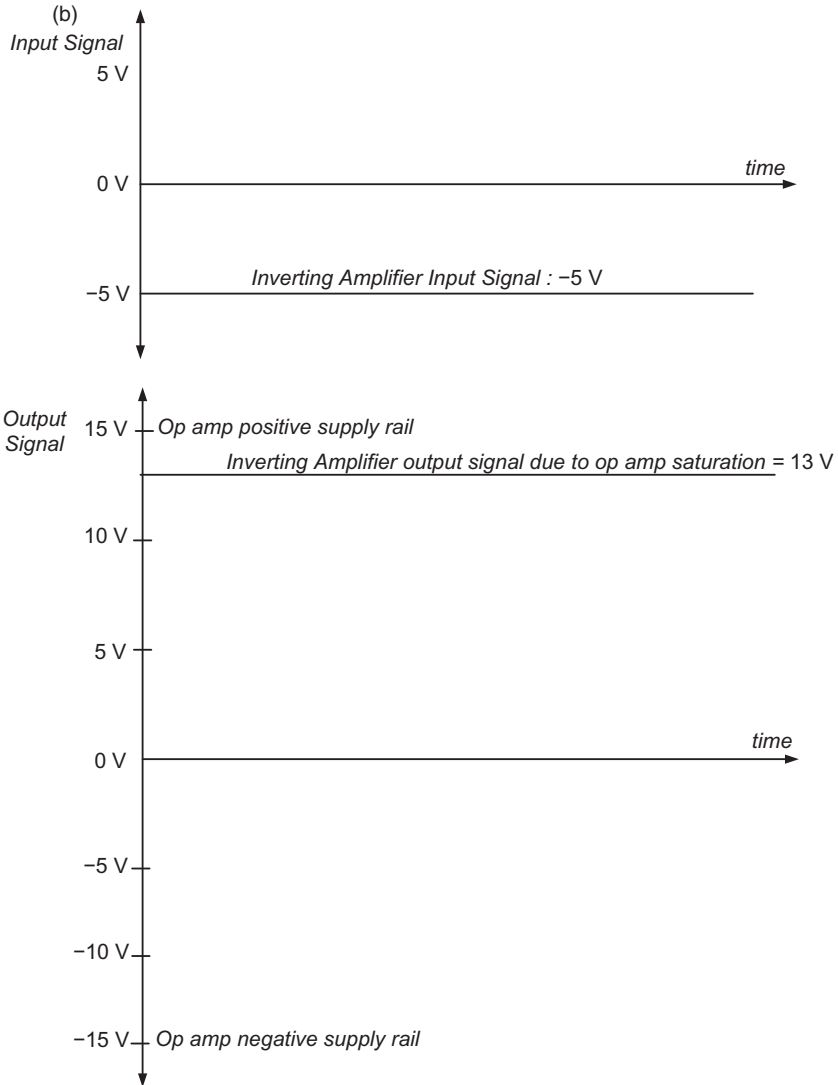
(b)
*Input Signal*

5 V

*time*

0 V

*Inverting Amplifier Input Signal : −5 V*

−5 V

*Output Signal*    15 V — *Op amp positive supply rail*

*Inverting Amplifier output signal due to op amp saturation* = 13 V

10 V

5 V

*time*

0 V

−5 V

−10 V

−15 V — *Op amp negative supply rail*

**Figure 5.6**    (*Continued*)

to implement. When the input times the amplifier gain exceeds the maximum voltage that the op amp can produce at its output, which is +15 V − 2 V = 13 V for positive outputs and when the op amp output is less than −15 V − (−2 V) = −13 V, the output of the op amp is clipped. This means that the output will never be over +13 V or be below −13 V. Referring again to Figure 5.6c, note that the clipped sinusoidal output waveform is a sinusoidal up until the clipping voltage limits are reached by the output. Such limits are
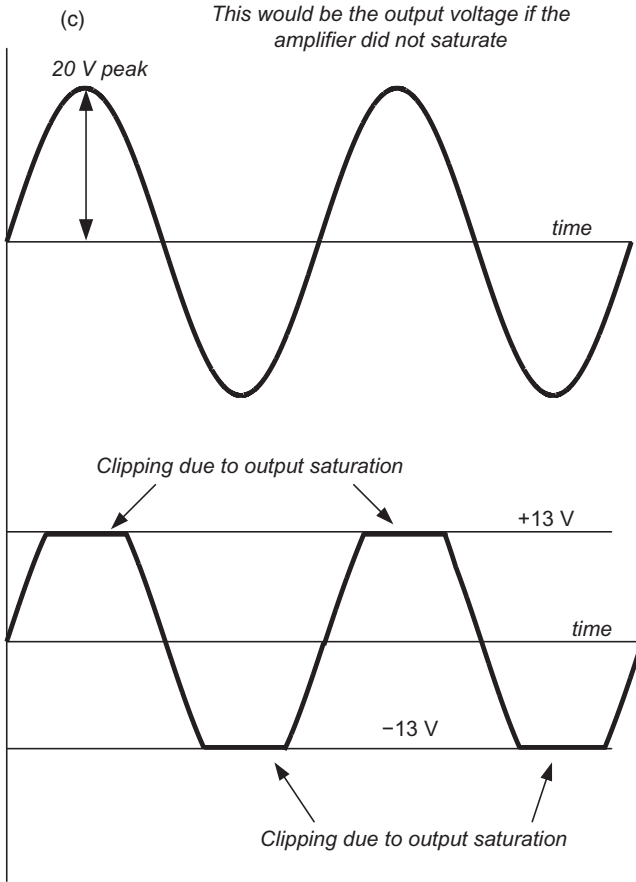
**Figure 5.6**  (*Continued*)

±13 V. Note that the top part of Figure 5.6c depicts the output as if the inverting amplifier could reproduce it with a linear gain of −4. The lower portion of Figure 5.6c shows what actually happens to the output because of the op amp saturation. This effect is called clipping and causes a usually undesired nonlinearity. Note: Figure 5.6c ignores the inverting sign of the CLG for simplicity.

Note that in all three cases, the maximum signal value times −4, the inverting gain of the amplifier, leads to a voltage of −20 V DC for case (a), +20 V DC for case (b), and −20 sin (2π 1 kHz) for (c). However, in all three cases, the inverting amplifier op amp output cannot go beyond ±13 V.

Figure 5.7 shows the same inverting amplifier of a gain of −4 V, when a sinusoidal signal of 3 sin (2π 1 kHz) gets well amplified by a factor of −4 without any clipping or distortion.

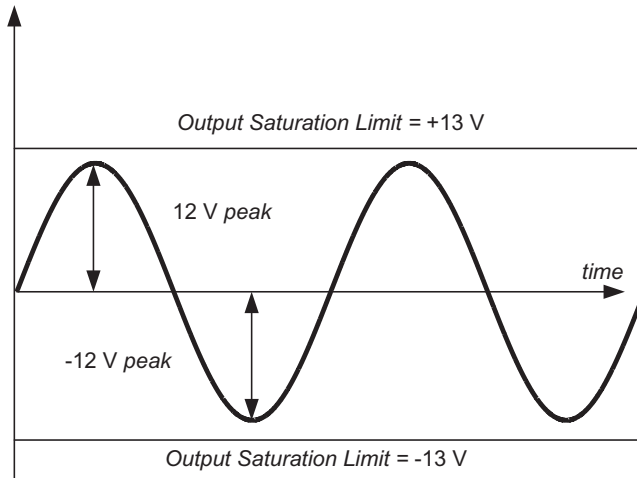The output waveform in Figure 5.7 does not saturate on either positive or negative cycles.

**Figure 5.7**  Inverting amplifier with a sinusoidal input that does not cause the op amp to saturate.

The 3 V peak input sinusoidal waveform is not shown in Figure 5.7. Since the inverting amp gain is –4 V, the magnitude of the positive and negative peaks of the output do not exceed ±12 V.

### 5.4.1.1.2  *Powering and Decoupling the Op Amp-Based with Positive and Negative Supplies*   Most op amps require two-polarity power supplies. Only special op amps require a single polarity supply. Figure 5.8 shows the interconnection required for two 15-V power supplies for the op amp to effectively see a +15 V at its +VDD power pin and –15 V at its –VDD power pin. In addition to the power supplies, the op amp requires what is usually referred to as decoupling capacitors. Decoupling capacitors need to be placed very near the op amp power pins, to eliminate any stray inductance on the wire leads. It is the decoupling capacitors that keep the voltage across the op amp power pins constant and without electrical noise. When the output or inputs of the op amp make transitions, the power supply cannot instantaneously supply the ±15-V power that the op amp requires at all times to operate correctly. The instantaneous voltage during such time is supplied for a short time by the decoupling capacitors, until the power supplies have time to respond to the transient.

*What value of decoupling capacitor we need?* As usual we need to make some assumptions about the situation, if that is not already given to us. Assume the power supplies can respond to the changes in power supply current demand in 1 ms, but no sooner than that. Then we have to size the $\pm V_{DD}$ decoupling capacitors to hold voltage level of the supplies constant for at least 1 ms at not less than the normal $V_{DD}$ value minus 100 mV. Also assume that the operational amplifier requires at most 10 mA of current of each of its supplies. However, the capacitor will not be able to maintain strictly a constant voltage.
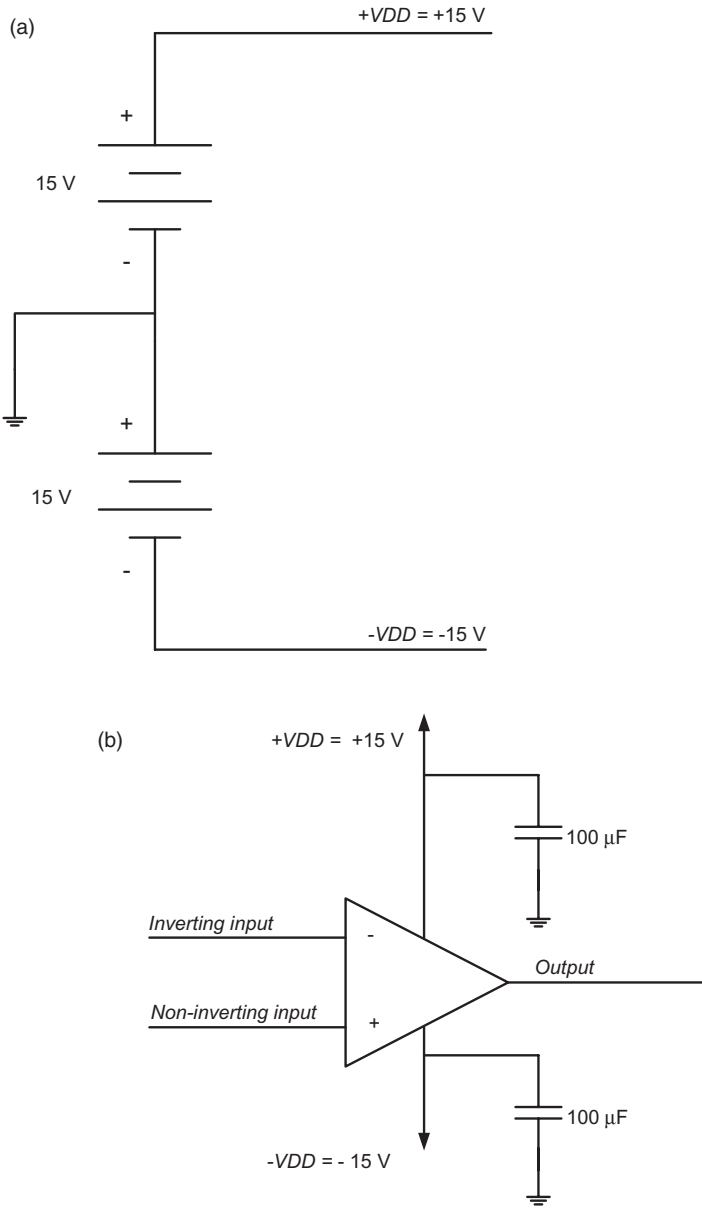
**Figure 5.8** Op amp power (a) $+V_{DD}$ and $-V_{DD}$, (b) decoupling capacitors.

As time passes, the decoupling voltage across each capacitor will droop a little bit. Why? The voltage–current relationship that governs the electrical behavior of a capacitor is

$$i(t) = C \, dv(t) / dt. \tag{5.18}$$

So let us use Equation (5.18) to calculate a capacitor value that will hold the voltage to 100 mV or less for 1 ms. Plugging in the numbers into Equation (5.18) and replacing differentials by finite increments we obtain

$$i(t) = C \, \Delta v(t) / \Delta t, \tag{5.19}$$

where

$$C = i(t)\Delta t / \Delta v(t) \tag{5.20}$$

$$C = 0.010 \times 0.001 / 0.1 = 100 \ \mu F. \tag{5.21}$$

Figure 5.8a depicts the generation of $+V_{DD}$ and $-V_{DD}$, and Figure 5.8b shows the 100 μF decoupling capacitors just calculated, connected to the op amp power supply pins.

Note that the other terminal of each capacitor not connected to a power supply rail, connects to ground.

After the charge of the capacitors is depleted, so that they would not be able to continue to supply the 15 V less 100 mV, the power supply is ready to supply current again and not only powers the op amp at this time, but also recharges the decoupling capacitors.

### 5.4.2 The Noninverting Amplifier

An op amp-based noninverting amplifier circuit is shown in Figure 5.9.

Let us point out the similarities and differences that exist between this circuit and the inverting amplifier of Figure 5.4. Both amplifiers have negative feedback. Note that on both amplifiers, the output voltage is sampled and fed back into the inverting input. The noninverting amplifier, however, has the input voltage $V_1$ applied to the positive or noninverting input; this is not the case for the inverting amplifier. Assuming that the op amp is ideal, we will calculate the output to input voltage ratio or the closed-loop transfer function of the noninverting amplifier. Remember that our ideal amplifier, however, requires power, and it will saturate if the output gets too close to either supply rail.

Node $A$ is virtually close to input voltage $V_1$, because the amplifier uses negative feedback and $\Delta V$ is practically zero; the voltage at node $A$ is $V_1$. So, by inspection of Figure 5.9, we have
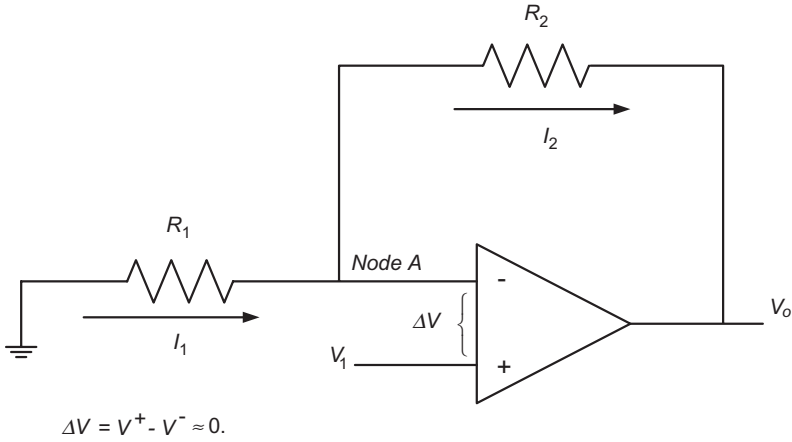
$$I_1 = -V_1 / R_1 \tag{5.22}$$

**Figure 5.9**   Noninverting amplifier.

and

$$V_1 - V_o = I_2 R_2. \tag{5.23}$$

Now, since there is no current entering or exiting the op amp inverting terminal,

$$I_1 = I_2. \tag{5.24}$$

Combining Equations (5.22) through (5.24) yields

$$\frac{V_o}{V_1} = 1 + \frac{R_2}{R_1}. \tag{5.25}$$

Equation (5.25) is the approximated transfer function of the closed loop gain of the noninverting amplifier. It is approximated because ideal op amp parameters have been assumed (Table 5.1). Note that the sign of the output matches the sign of the input waveform. Additionally, it is important to note that the CLG $(1 + R_2/R_1)$ is always strictly greater than one if both resistors are greater than 0 $\Omega$. The noninverting amplifier ±input signal times the CLG $(1 + R_2/R_1)$ must be less than the absolute value of the power supply rail.

**Example 5.4**   Given a noninverting amplifier like the one shown in Figure 5.9, assuming that the op amp is ideal, but with an op amp $V_{SAT} = \pm 13$ V, and input $V_1$ is ±1 V maximum, determine the maximum CLG of the noninverting amplifier that will not allow the output to become saturated. Assume ±15 V power supplies.

Solution: Since the closed loop of the noninverting amplifier is: $(1 + R_2/R_1)$, the supply rail is +15 V, and $V_{SAT} = 13$ V, the maximum positive and negative swings that the amplifier can have is ±13 V. Note that this amplifier will only swing to the negative voltage rail if the input is negative.

$$\pm 13 \text{ V} / 1 \text{ V} = \pm 13. \tag{5.26}$$

Then using Equation (5.26) with Equation (5.25) we have

$$\pm V_o / V_1 = 1 + \frac{R_2}{R_1} = \pm 13. \tag{5.27}$$

From Equation (5.17) we determine that the $R_2/R_1$ ratio must equal 12. So for example $R_2 = 12 \text{ } k\Omega$ and $R_1 = 1 \text{ } k\Omega$.

### 5.4.2.1    Effects of Finite Op Amp Open-Loop Gain in the Closed-Loop Equation of the Noninverting Amplifier
In a very similar manner as it was done with the inverting amplifier configuration assuming a finite open-loop gain op amp model, we arrive at the noninverting amplifier CLG which is:

$$V_o / V_1 = \frac{1 + R_1 / R_2}{1 + \dfrac{1}{A_{OL}}(1 + R_1 / R_2)}. \tag{5.28}$$

The op amp circuit model used to derive Equation (5.28) is given by the circuit of Figure 5.10 where $A_{OL}$ is assumed to be finite.
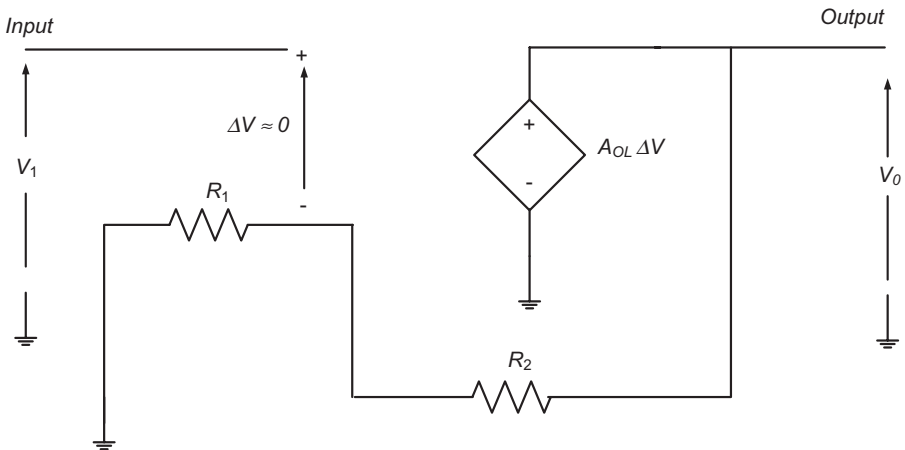


**Figure 5.10**    Model of noninverting amplifier with finite $A_{OL}$.

**Table 5.4   Noninverting amplifier closed-loop gain (CLG) errors for finite $A_{OL}$: for an estimated CLG of 2**

| Finite Op Amp Open-Loop Gain ($A_{OL}$) | Op Amp $A_{OL}$ in dB | Closed-Loop Gain of 2 (CLG = 2) with Finite $A_{OL}$ | CLG = 2 Absolute Error | CLG = 2 Relative Error |
|---|---|---|---|---|
| (V/V) | (dB) | (V/V) | (V/V) | (%) |
| 1 | 0 | 1.333333 | 0.666667 | 50.000000 |
| 10 | 20 | 1.833333 | 0.166667 | 9.090909 |
| 100 | 40 | 1.980392 | 0.019608 | 0.990099 |
| 1,000 | 60 | 1.998004 | 0.001996 | 0.099900 |
| 10,000 | 80 | 1.999800 | 0.000200 | 0.009999 |
| 100,000 | 100 | 1.999980 | 0.000020 | 0.001000 |
| 1,000,000 | 120 | 1.999998 | 0.000002 | 0.000100 |
| 10,000,000 | 140 | 2.000000 | 0.000000 | 0.000010 |

**Table 5.5   Noninverting amplifier closed-loop gain (CLG) errors for finite $A_{OL}$: for an estimated CLG of 20**

| Finite Op Amp Open-Loop Gain ($A_{OL}$) | Op Amp $A_{OL}$ in dB | Closed-Loop Gain of 20 (CLG = 20) with Finite $A_{OL}$ | CLG = 20 Absolute Error | CLG = 20 Relative Error |
|---|---|---|---|---|
| (V/V) | (dB) | (V/V) | (V/V) | (%) |
| 1 | 0 | 0.952381 | 19.047619 | 2,000.000000 |
| 10 | 20 | 6.666667 | 13.333333 | 200.000000 |
| 100 | 40 | 16.666667 | 3.333333 | 20.000000 |
| 1,000 | 60 | 19.607843 | 0.392157 | 2.000000 |
| 10,000 | 80 | 19.960080 | 0.039920 | 0.200000 |
| 100,000 | 100 | 19.996001 | 0.003999 | 0.020000 |
| 1,000,000 | 120 | 19.999600 | 0.000400 | 0.002000 |
| 10,000,000 | 140 | 19.999960 | 0.000040 | 0.000200 |

Using Equation (5.25) as the estimated value of the CLG and Equation (5.28) as the true value of the CLG for an op amp with finite open-loop gain $A_{OL}$, we can calculate the absolute and relative errors of the noninverting amplifier CLG equation when the op amp $A_{OL}$ is finite.

Tables 5.4 and 5.5 show the errors that exist for a noninverting amplifier configuration for CLGs of 2 and 20 for various values of $A_{OL}$.

### 5.4.3   The Buffer or Noninverting Amplifier of Unity Gain

The buffer amplifier is a special case of the noninverting amplifier. Referring to the circuit in Figure 5.9, if $R_2$ approaches 0 and $R_1$ approaches infinity, then $V_o = V_1$.

For the reader's convenience, we repeat the gain equation of the noninverting amplifier given by Equation (5.25):

$$\frac{V_o}{V_1} = 1 + \frac{R_2}{R_1}.$$ (5.29)

Expressing $V_o$ as a function of $V_1$ and resistors $R_1$ and $R_2$, and taking the limit of the expression for $R_1 \to \infty$ and $R_2 \to 0$, we obtain

$$\lim_{\substack{R_1 \to \infty \\ R_2 \to 0}} V_o = (1 + R_2 / R_1)V_1 = V_1.$$ (5.30)

Figure 5.11a depicts a unity gain noninverting amplifier or simply a buffer.

So what is the meaning of $V_o = V_1$? Literally, it means that the output voltage is equal to the input voltage. If we connect just a wire between $V_1$ and $V_0$ without having any op amp in between, we get the same voltage relationship. To explain the importance of the circuit of Figure 5.11a we need to assume that the idealized input resistance of the op amp is actually finite and not infinite like it is for the ideal op amp model. Additionally, we will assume that the op amp $A_{OL}$ is also finite. This op amp model described with finite input resistance and open-loop gain is presented in Figure 5.11b and the buffer amplifier, using the op amp model from Figure 5.11b, is shown in Figure 5.11c

Writing the Kirchhoff equations for the circuit of Figure 5.11c and realizing that

$$V_1 - V_o = V_1 - A_{OL}(V_1 - V_o),$$

we find that

$$A_{CL} = V_o / V_1 = A_{OL} / (A_{OL} + 1) \approx 1$$ (5.31)

$$R_{inCL} = (A_{OL} + 1)R_{in} \approx A_{OL}R_{in}.$$ (5.32)

$A_{CL}$ is the CLG of the buffer amplifier and $R_{inCL}$ is the closed-loop input resistance of the buffer amplifier. Because for a buffer amplifier the input voltage is quite approximately equal to the output voltage, Equation (5.31), this amplifier is also called a *voltage follower*.

$R_{in}$ is the op amp input resistance, usually of several mega-ohms. $A_{OL}$ is the op amp open-loop gain. $R_{inCL}$ stands for the closed-loop input resistance of the buffer amplifier, not the op amp input resistance.

From Equation (5.32) it is clear to see that since $R_{in}$ is in the order of several mega-ohms, $A_{OL}$ is in the order of $10^6$ V/V, the closed-loop input resistance of the buffer amplifier configuration (see Figure 5.11c) is in the order of $10^{12}$ $\Omega$. The closed-loop input resistance of the buffer amplifier is the effective resistance that the input $V_1$ sees at the noninverting input terminal of the amplifier.
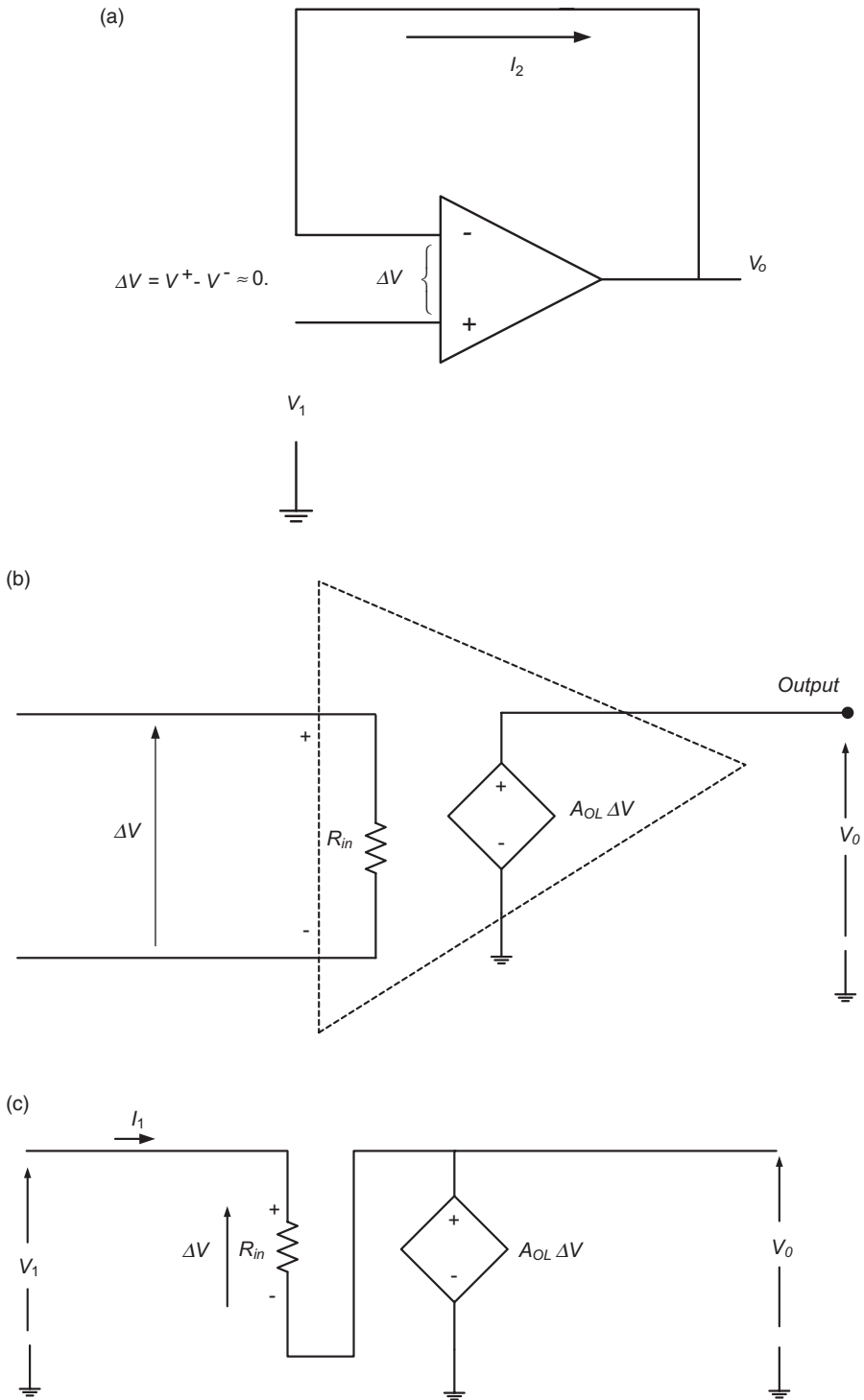
(a)

$I_2$

$-$

$\Delta V$

$+$

$V_o$

$\Delta V = V^+ - V^- \approx 0.$

$V_1$

(b)

*Output*

$+$

$\Delta V$

$R_{in}$

$+$

$-$

$A_{OL}\, \Delta V$

$V_0$

(c)

$I_1$

$+$

$\Delta V$ $R_{in}$

$-$

$+$

$-$

$A_{OL}\, \Delta V$

$V_1$

$V_0$

**Figure 5.11** (a) Buffer amplifier, (b) op amp with model finite $R_{in}$ and $A_{OL}$, (c) actual buffer amplifier circuit using the model from part (b).

So for input signals in the order of 1 V, the current drawn by the buffer ampli-
fier is in the order of pico amps ($10^{-12}$ A)!

Based on what we just discussed, the buffer amplifier, which operates as a
unity gain noninverting amplifier, is in effect a current amplifier. The output
of the buffer circuit is converted to a voltage with much higher drive capability
than the pico amp input current. It can also be proven from the circuit of
Figure 5.11c by adding a finite (nonzero) $R_{out}$ between the plus sign of the $A_{OL}$
$\Delta_V$-controlled source and the output voltage $V_o$, that the effective output resis-
tance of the buffer amplifier is

$$R_{outCL} = \frac{R_{out}}{(1 + A_{OL})},$$ (5.33)

where $R_{out}$ is the op amp output resistance, which we have assumed to be zero
in the ideal op amp model. In a real op amp, $R_{out}$ is larger than zero and typi-
cally is a small fraction of an ohm to a few ohms. $R_{outCL}$ is the effective output
resistance that the buffer amplifier presents to a load that can be connected
at its output. Let us consider the following numerical example to quantify the
significance of finite $R_{in}$ and finite $A_{OL}$.

**Example 5.5** The circuit of Figure 5.12a consists of a resistor divider formed
with $R_1$ and $R_2$. The intent of this resistor divider is to provide 5 V to any load.
This will only work with some accuracy if the load resistance is much higher
than 1 kΩ. But in the circuit example the load resistance is also 1 kΩ. The load
has a loading effect on the 5 V at node A of the resistor divider. After stating
the circuit Kirchhoff equations and solving them we determine that the voltage
across $R_{LOAD}$ is 3.333 V, this is considerably lower than the desired 5 V. Figure
5.12b shows the circuit divider circuit to which a buffer amplifier configuration
was added to right side of node $A$. The output of the buffer drives $R_{LOAD}$. Since
the buffer does not draw any significant current from the resistor divider, the
buffer supplies to $R_{LOAD}$ practically the 5 V at the input of the buffer to $R_{LOAD}$.
The advantage of this circuit (Fig. 5.12b) is that for load resistances much
larger than 1 kohm, the op amp-based buffer can supply the current required
by the load. To continue to work with this example, consider the circuit of
Figure 5.12a and calculate the voltage at $R_{LOAD}$, when $R_{LOAD} = 1$ Ω, 100 Ω,
10 kΩ, 100 kΩ, and 1 MΩ, refer to Table 5.6 for the numerical answers of this
example.

By Kirchhoff, the voltage at node $A$ is

$$V_A = \frac{V_{input} \cdot (R_2 // R_{LOAD})}{R_1 + (R_2 // R_{LOAD})}.$$ (5.34)

Plugging into Equation (5.34) 1 Ω, 100 Ω, 10 kΩ, 100 kΩ, and 1 MΩ we obtain
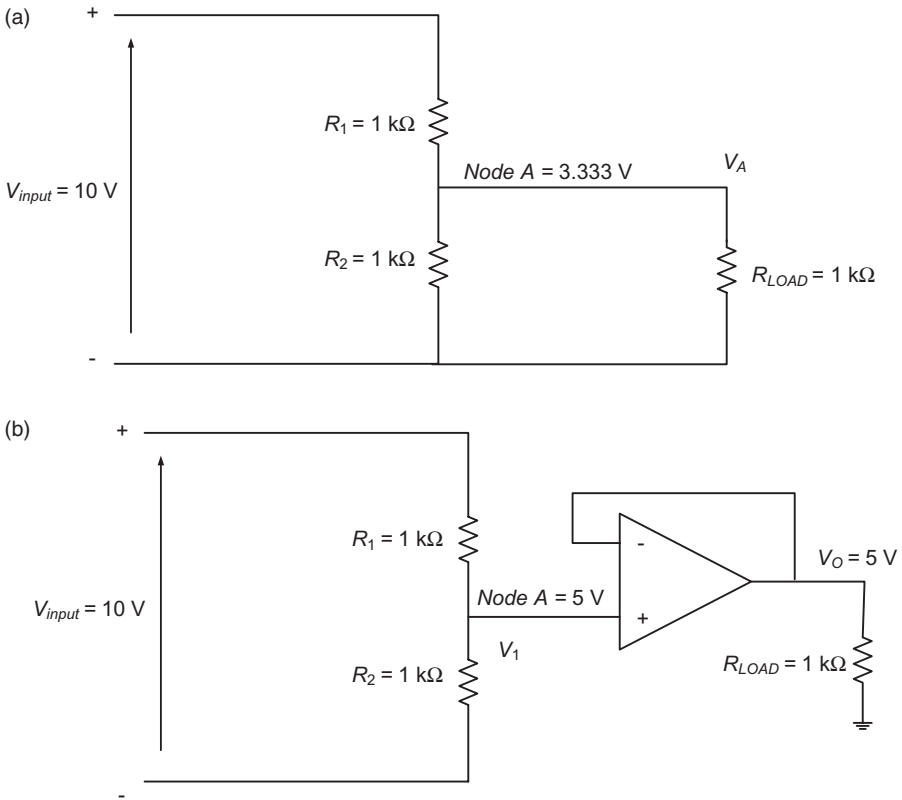Table 5.6.

**Figure 5.12** (a) Resistor divider loaded with a resistor at node *A* and no buffer amplifier, (b) resistor divider load with a resistor after buffering node *A*, with a voltage follower.

**Table 5.6    Load effect on circuit without and with buffering op amp**

| $R_{LOAD}$ ($\Omega$) | $V_A$ (V); Figure 5.12a without Op Amp | $V_o$ (V); Figure 5.12b with Op Amp |
|---|---|---|
| 1 | 0.00998004 | 5.0 |
| 100 | 0.098039216 | 5.0 |
| 10,000 | 4.761904762 | 5.0 |
| 100,000 | 4.975124378 | 5.0 |
| 1,000,000 | 4.997501249 | 5.0 |

It is interesting to note that the larger the load resistance value is with respect to the values of the resistor dividers, when no buffer amplifier is used, then the better is the output voltage accuracy. For instance, for 1 M$\Omega$ load resistance, without using a buffer amp, the voltage across the load is quite close to 5 V. For 1 $\Omega$, that is not the case; that is, 0.00998004 V is much lower when compared against the 5 V obtained using the buffer amplifier.
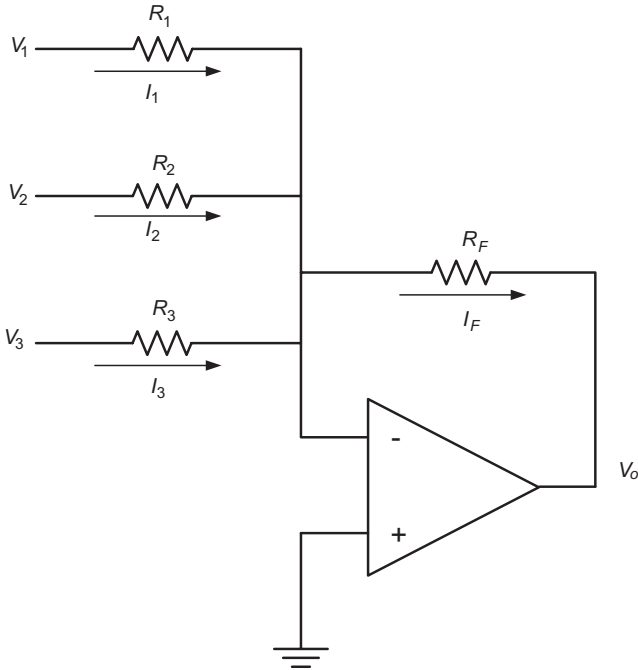
**Figure 5.13**   Three-input inverting adder amplifier.

### 5.4.4   The Inverting Adder

Figure 5.13 shows the circuit topology of an inverting adding amplifier. We only show a three-input circuit; however; the circuit can easily be generalized to *n*-inputs, where *n* is an integer. Let us analyze this circuit to determine the output voltage as a function of all the circuit resistors and the input voltages. We will do the analysis assuming that the op amp is ideal.

Since the op amp is ideal and the circuit has negative feedback, the voltage difference across the inverting and noninverting inputs of the op amp is zero $(\Delta V = V^+ - V^- = 0)$.

Additionally, since the input resistance of the op amp is infinite and using KCL we have that

$$I_1 + I_2 + I_3 = I_F. \qquad (5.35)$$

Now since the negative input of the op amp is virtually grounded, we have using Equation (5.35) and applying Ohms law to each circuit branch:

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_o}{R_F}. \qquad (5.36)$$

Doing some algebra on Equation (5.36) we obtain

$$V_o = -R_F \left( \frac{1}{R_1} V_1 + \frac{1}{R_2} V_2 + \frac{1}{R_3} V_3 \right). \qquad (5.37)$$

We usually prefer to make $R_1 = R_2 = R_3 = R$ so that Equation (5.37) becomes

$$V_o = -\frac{R_F}{R} (V_1 + V_2 + V_3). \qquad (5.38)$$

Equation (5.38) is also referred to as the inverting adder with constant gain output voltage, since the ratio $R_F/R$ is the same for all the inputs. When the input signals are audio frequency signals, the circuit is also called an *audio mixer*.

**Example 5.6**  Derive the output voltage equation of an *n*-input inverting adder with constant gain circuit. Assume the op amp is ideal.

Proceeding just like we did to obtain Equations (5.36)–(5.38), we simply generalize them to have *n*-inputs and obtain the following:

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \cdots + \frac{V_n}{R_n} = -\frac{V_o}{R_F} \qquad (5.39)$$

$$V_o = -R_F \left( \frac{1}{R_1} V_1 + \frac{1}{R_2} V_2 + \frac{1}{R_3} V_3 + \cdots + \frac{1}{R_n} V_n \right). \qquad (5.40)$$

We usually prefer to make $R_1 = R_2 = R_3 = \cdots = R_n = R$ so that Equation (5.40) becomes

$$V_o = -\frac{R_F}{R} (V_1 + V_2 + V_3 + \cdots + V_n). \qquad (5.41)$$

*Important note about inverting adders of any number of inputs:*
In order for the inverting adder circuit to operate linearly and without saturation, it is required that

$$|V_{SAT}| > \left| R_F \left( \frac{1}{R_1} V_1 + \frac{1}{R_2} V_2 + \frac{1}{R_3} V_3 + \cdots + \frac{1}{R_n} V_n \right) \right|. \qquad (5.42)$$

And when $R_1 = R_2 = R_3 = \cdots = R_n = R$, then

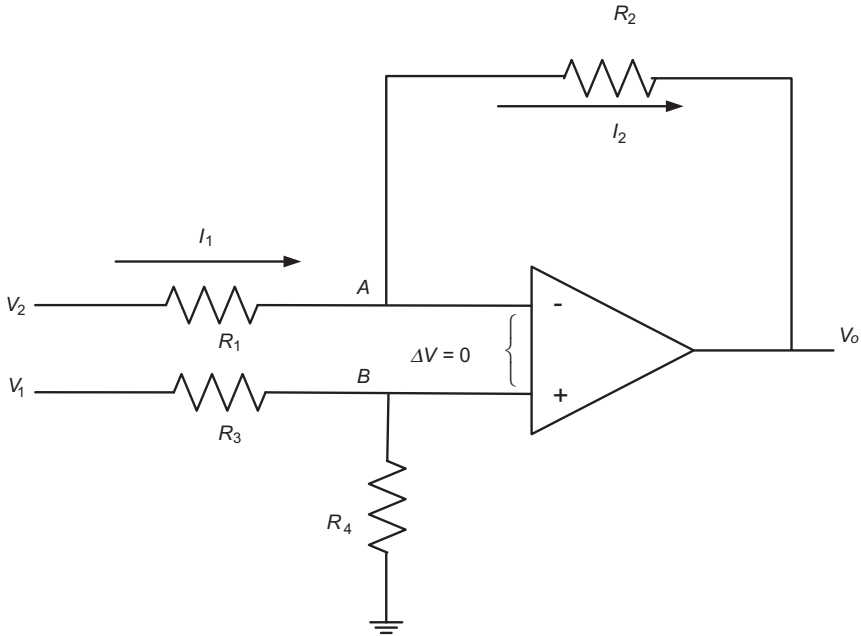$$|V_{SAT}| = \left| \frac{R_F}{R} (V_1 + V_2 + V_3 + \cdots + V_n) \right|.$$

**Figure 5.14**   Op amp-based difference amplifier.

### 5.4.5   The Difference Amplifier

Figure 5.14 shows the circuit of an op amp-based difference amplifier. Let us analyze the circuit to calculate the output to inputs relationship of this amplifier.

First, let us note that the op amp has negative feedback, like all previous configurations did. The feedback is negative because the output is sampled and injected back into the inverting terminal of the op amp. Then assuming our op amp is ideal and since it has negative feedback, the $\Delta V$ or the voltage difference between the noninverting and inverting inputs is infinitely small or practically zero.

By inspection of Figure 5.14 we see that $\Delta V$, which is the difference between node voltages $B$ and $A$, is practically zero. So the voltage at node $A$ is identical to the voltage at node $B$. We will refer to this voltage as $V_A$. Moreover, it is easy to see that

$$V_A = V_B = \frac{R_4}{R_3 + R_4} V_1.$$
(5.43)

The current that flows through resistor $R_1$ is

$$I_1 = (V_2 - V_A)/R_1.$$
(5.44)

Plugging the value of $V_A$ from Equation (5.43) into Equation (5.44) we obtain

$$I_1 = \frac{V_2 - \dfrac{R_4}{R_3 + R_4} V_1}{R_1}. \tag{5.45}$$

Current $I_2$ through resistor $R_2$ is

$$I_2 = (V_A - V_o) / R_2. \tag{5.46}$$

Again plugging the value of $V_A$ from Equation (5.43) into Equation (5.46) we obtain

$$I_2 = \frac{\dfrac{R_4}{R_3 + R_4} V_1 - V_0}{R_2}. \tag{5.47}$$

Since $I_1 = I_2$, equating Equations (5.45) and Equation (5.47) we get

$$\frac{V_2 - \dfrac{R_4}{R_3 + R_4} V_1}{R_1} = \frac{\dfrac{R_4}{R_3 + R_4} V_1 - V_0}{R_2}. \tag{5.48}$$

Carefully doing the algebra on Equation (5.48) we obtain the output of the difference amplifier as a function of its two input voltages and resistors $R_1$ through $R_4$:

$$V_o = \left( \frac{R_1 + R_2}{R_1} \right) \left( \frac{R_4}{R_3 + R_4} \right) V_1 - \frac{R_2}{R_1} V_2. \tag{5.49}$$

Equation (5.49) is the difference amplifier transfer function when all resistors ($R_1$ through $R_4$) are different in value. Additionally, Equation (5.49) is the expression of the difference amplifier gain when the op amp is assumed to be ideal.

Ideal difference amplifiers only amplify the difference of the two input signals and fully reject the average of the sum of the two input signals, also referred to as the common mode input signal. This means that Equation (5.50) is nonzero and Equation (5.51) is zero for an ideal op amp-based difference amplifier.

$$\textit{Differential input signal}: V_{idiff} = V_1 - V_2 \tag{5.50}$$

$$\textit{Common mode input signal}: V_{icm}\ \tfrac{1}{2}(V_1 + V_2). \tag{5.51}$$

However, in the real world, difference amplifiers will not only amplify the differential mode input signal, but also the common mode signal to some extent.

The following equation is an expression of the output voltage produced by the presence of both types of gains, the differential and the common mode:

$$V_o = A_{diff} V_{idiff} + A_{cm} V_{icm}. \tag{5.52}$$

It is important to note that the difference amplifier of Figure 5.14 is nonideal even if it is implemented with an ideal operational amplifier. Why is this so? Because a real difference amplifier, regardless of using an ideal or a real op amp, has both differential and common mode gains that are not zero. The common mode gain is different from zero due greatly to the resistor inaccuracies. Using the circuit of Figure 5.14 we can calculate the value of the common mode gain by injecting an input of the same polarity to both the inverting and noninverting inputs of the difference amplifier. Figure 5.15 depicts the combined input signal to determine the difference amplifier common mode gain.

If the op amp used for the difference amplifier is ideal, again we have that the $\Delta V$ is zero, that is, node $A$ and node $B$ are at the same voltage level; however, the voltage at node $A$ (and $B$) is not zero. Again making the usual assumptions about ideal op amps, we calculate the voltage at node $B$, as the one produced by the common mode input voltage $V_{icm}$ and the resistor divider formed by $R_3$ and $R_4$ (Fig. 5.15):
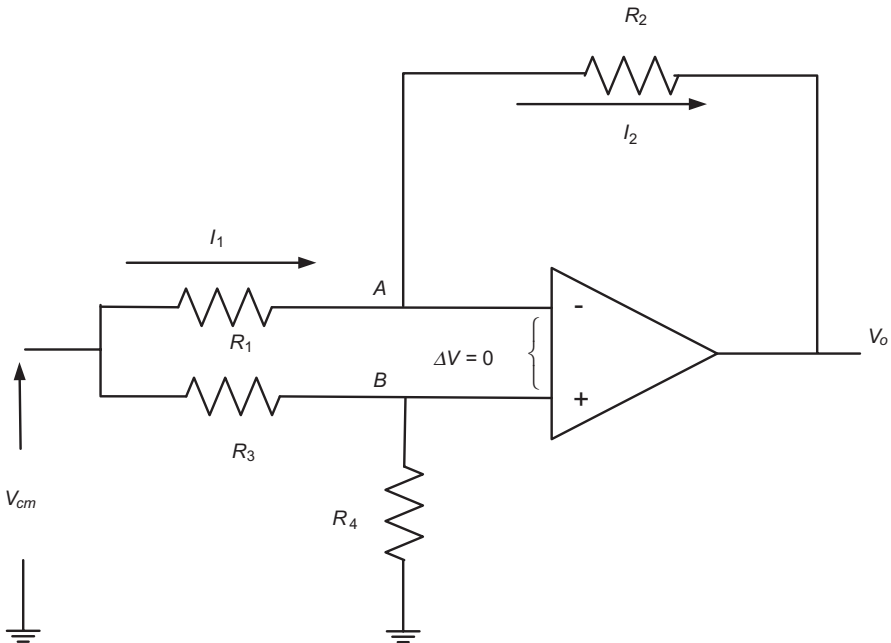


**Figure 5.15** Common mode input signal to determine the difference amplifier common mode gain.

$$V_A = V_B = V_{cm}\left(\frac{R_4}{R_3 + R_4}\right). \tag{5.53}$$

From the circuit of Figure 5.15 we see that

$$I_1 = \frac{V_{cm} - V_A}{R_1}. \tag{5.54}$$

Plugging Equation (5.53) into Equation (5.54) we obtain

$$I_1 = \frac{V_{cm} - \dfrac{R_4}{R_3 + R_4} V_{cm}}{R_1}. \tag{5.55}$$

We also have that

$$I_2 = \frac{\dfrac{R_4}{R_3 + R_4} V_{cm} - V_o}{R_2}. \tag{5.56}$$

And since $I_1 = I_2$, we get

$$\frac{V_{cm} - \dfrac{R_4}{R_3 + R_4} V_{cm}}{R_1} = \frac{\dfrac{R_4}{R_3 + R_4} V_{cm} - V_o}{R_2}. \tag{5.57}$$

Doing some algebra on Equation (5.57) and expressing everything in terms of $V_o/V_{cm}$ we get

$$\frac{V_o}{V_{cm}} = \frac{R_3}{R_3 + R_4}\left(1 - \frac{R_2}{R_1}\frac{R_3}{R_4}\right). \tag{5.58}$$

Equation (5.58) is the equation of the common mode gain of the difference amplifier.

Since we want a difference amplifier to have a zero common mode gain, so that it amplifies only differential signals and it eliminates common mode input signals. For the common mode gain to be zero, the right-hand side term of Equation (5.58) needs to be zero. This is achieved by having the following resistor ratios:

$$\frac{R_2}{R_1} = \frac{R_4}{R_3}. \tag{5.59}$$

When Equation (5.59) is met. the common mode gain of the difference amplifier with an ideal op amp becomes zero. Thus:

$$A_{cm} = \frac{V_o}{V_{cm}} = 0. \tag{5.60}$$

**Example 5.7**   Given a difference amplifier just like the one in Figure 5.14, determine the value of the differential mode gain, using Equation (5.52) as the condition that inhibits the common mode gain. Assume that the op amp is ideal.

So using the general expression for the difference amplifier gain from Equation (5.49), which we repeat here for the reader's convenience is

$$V_o = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right)V_1 - \frac{R_2}{R_1}V_2. \tag{5.61}$$

Equation (5.61) consists of differential and common mode gains. Doing some algebraic manipulations on Equation (5.61) we obtain

$$V_o = \left(1 + \frac{R_2}{R_1}\right)\frac{1}{R_3}\frac{R_4}{1 + \frac{R_4}{R_3}}V_1 - \frac{R_2}{R_1}V_2. \tag{5.62}$$

Then, plugging the condition given by Equation (5.59) into Equation (5.62), we get an expression for the differential amplifier gain, rid of any common mode gain, thus:

$$V_o = \frac{R_2}{R_1}(V_1 - V_2). \tag{5.63}$$

Referring once more to Figure 5.14 note that $V_1$ is the input to the noninverting side of the difference amplifier, while $V_2$ is the input to the inverting side of the amplifier.

A closer look at Equation (5.63) reveals that the difference between $V_1$ and $V_2$ is amplified by the ratio of $R_2/R_1$. This ratio is called the difference amplifier gain. Remember that Equation (5.63) is valid when the condition given by Equation (5.59) is met.

Additionally, if

$$R_1 = R_2 = R_3 = R_4, \tag{5.64}$$

Equation (5.63) becomes

$$V_o = V_1 - V_2. \tag{5.65}$$

Equation (5.65) is the expression of the difference amplifier output voltage strictly as a function of the difference between voltages $V_1$ and $V_2$.
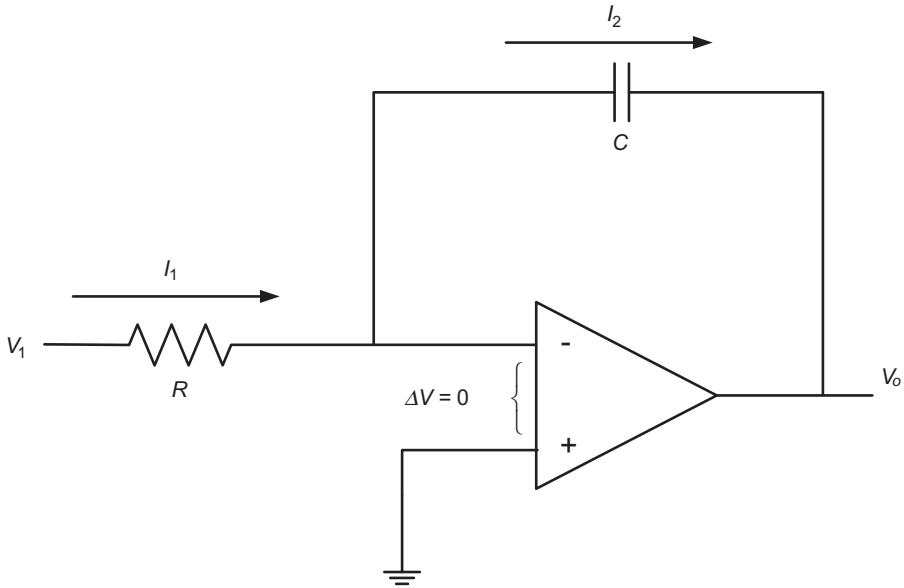
**Figure 5.16**  Pure integrator circuit using an ideal op amp.

### 5.4.6  The Inverting Integrator

If we have an inverting amplifier configuration and replace the resistor in the feedback loop with a capacitor, the circuit obtained is an integrator. Figure 5.16 depicts an integrator using an op amp. The output to input voltage ratio in the frequency domain is then

$$V_o / V_1 = -\frac{1/j\omega C}{R} = -\frac{1}{j\omega RC}. \tag{5.66}$$

In the time domain and referring to Figure 5.16 we have that

$$I_1 = I_2, \tag{5.67}$$

where

$$I_1 = V_1 / R \tag{5.68}$$

and

$$I_2 = -C\frac{dV_o}{dt}. \tag{5.69}$$

Combining Equations (5.67) through (5.69 yields

$$\frac{V_1}{R} = -C\frac{dV_o}{dt}.$$

(5.70)

Integrating Equation (5.70) and expressing the output voltage $V_o$, the following is obtained:

$$V_o = -\frac{1}{RC}\int V_1 dt.$$

(5.71)

The Bode plots of an integrator given by Equation (5.66) are shown in Figure 5.17.

The integrator design frequency is $f_o = 1/2\pi\,RC$ where $R$ and $C$ are the values of the resistor and capacitor of the integrator circuit shown in Figure 5.16. It is important to notice the difference between the op amp-based integrator of Figure 5.16 and the first order $RC$ LPF from Chapter 4, Figure 4.4. The op amp-based integrator has an infinite gain at DC or at zero frequency. The gain or magnitude decreases at a constant rate of 20 dB *per decade*. The first-order $RC$ LPF integrator circuit, which has no op amp, has a 0 dB gain at frequencies below the integrator $f_0$ cutoff frequency and the gain decays at a constant rate of 20 dB per decade above $f_0$. Refer to this previously discussed circuit Bode plots in Figure 4.4. So what does this all mean in terms of practical operation of the integration? The op amp-based integrator has an infinite gain at DC, so if the input signal to be integrated is constant, the op amp will saturate. That is the reason why op amp integrators implemented like in Figure 5.16 are not quite that practical. One needs to add a semiconductor switch in parallel with the capacitor to reset the op amp output by discharging the capacitor, to let the integration restart. Another issue with the op amp-based integrator of Figure 5.16 is that any noisy signals below the integrator $f_0$ frequency become amplified more than the integrated frequency. We will shortly address a practical integrating op amp-based circuit that performs better than the one being presented and does not have the deficiencies just mentioned. It is also important to mention that the circuit of Figure 5.16 has a constant phase shift of $-90°$ for all frequencies, whereas the first-order $RC$ integrator does not (refer to Figure 4.4).

### 5.4.7   The Inverting Differentiator

If we have an inverting amplifier configuration and replace the resistor in the input path with a capacitor, the circuit obtained is a differentiator. Figure 5.18 depicts a differentiator using an op amp. The output to input voltage ratio in the frequency domain is then
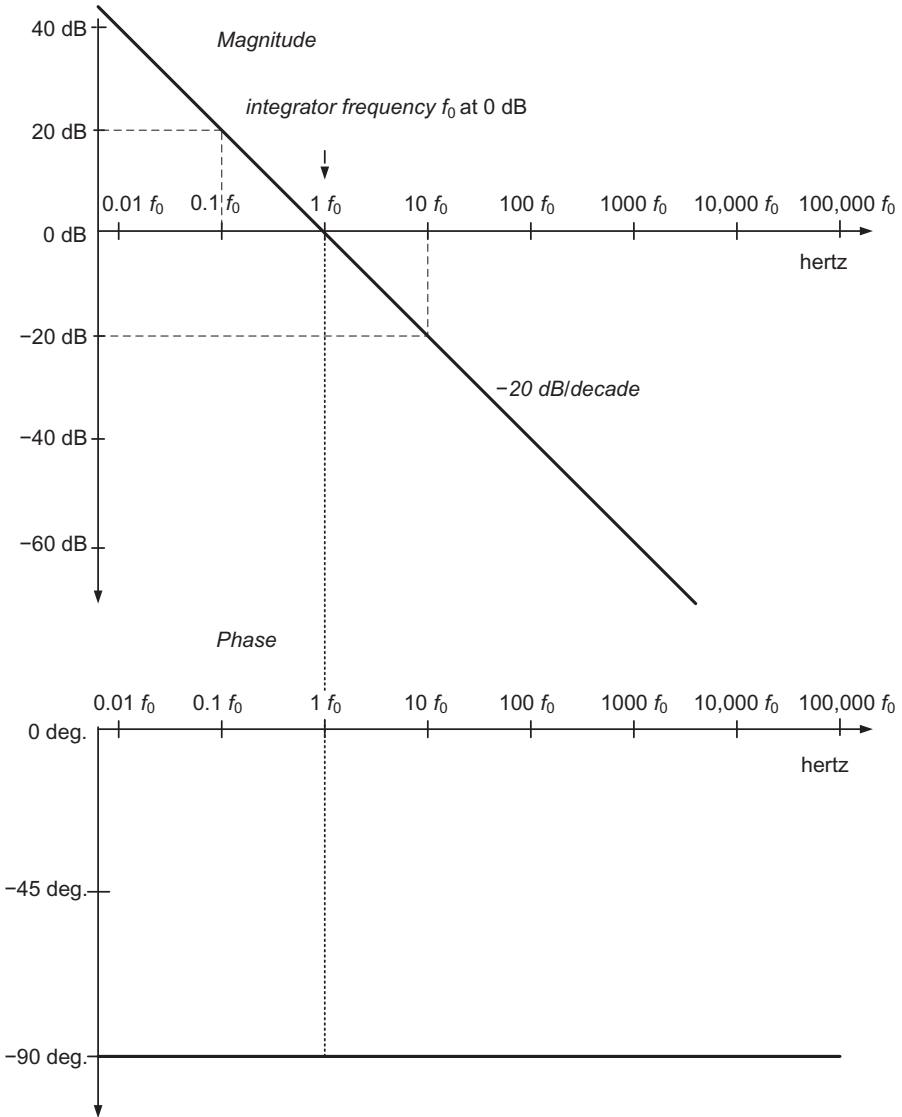
$$V_o / V_i = -j\omega RC.$$

(5.72)

**Figure 5.17** Op amp-based pure integrator asymptotic Bode plots.

In the time domain and referring to the differentiator of Figure 5.18 we have that

$$I_1 = I_2, \qquad (5.73)$$

where

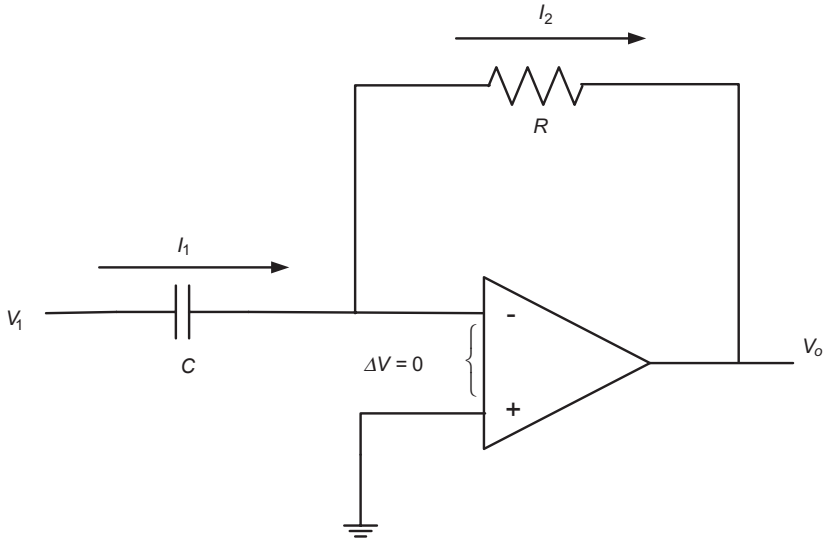$$I_1 = \frac{V_1}{\dfrac{1}{j\omega C}} \qquad (5.74)$$

**Figure 5.18**   Pure differentiator circuit using an ideal op amp.

and

$$I_2 = -\frac{V_o}{R}. \tag{5.75}$$

Combining Equations (5.74) and (5.75) according to Equation (5.73) it yields

$$\frac{V_o}{V_1} = -j\omega RC. \tag{5.76}$$

Equation (5.76) is the expression of a differentiator transfer function in the frequency domain. We will also determine the time domain equation of the differentiator output voltage. Again by referring to Figure 5.18 we see that $I_1 = I_2$. Since current $I_1$ through the capacitor is

$$I_1 = CdV_1 / dt \tag{5.77}$$

and

$$I_2 = -V_o / R. \tag{5.78}$$

Combining Equations (5.77) and (5.78) we obtain the expression of the output voltage for the inverting differentiator:

$$V_o = -RC\frac{dV_1}{dt}. \tag{5.79}$$

The Bode plots of a differentiator derived from the frequency domain Equation (5.76) are shown in Figure 5.19.

The differentiator frequency is $f_0 = 1/2\pi\, RC$ where $R$ and $C$ are the values of the resistor and capacitor of the differentiator circuit shown in Figure 5.18. It is important to notice the difference between the op amp-based differentiator of Figure 5.18 and the first-order $RC$ HPF differentiator from Chapter 4,
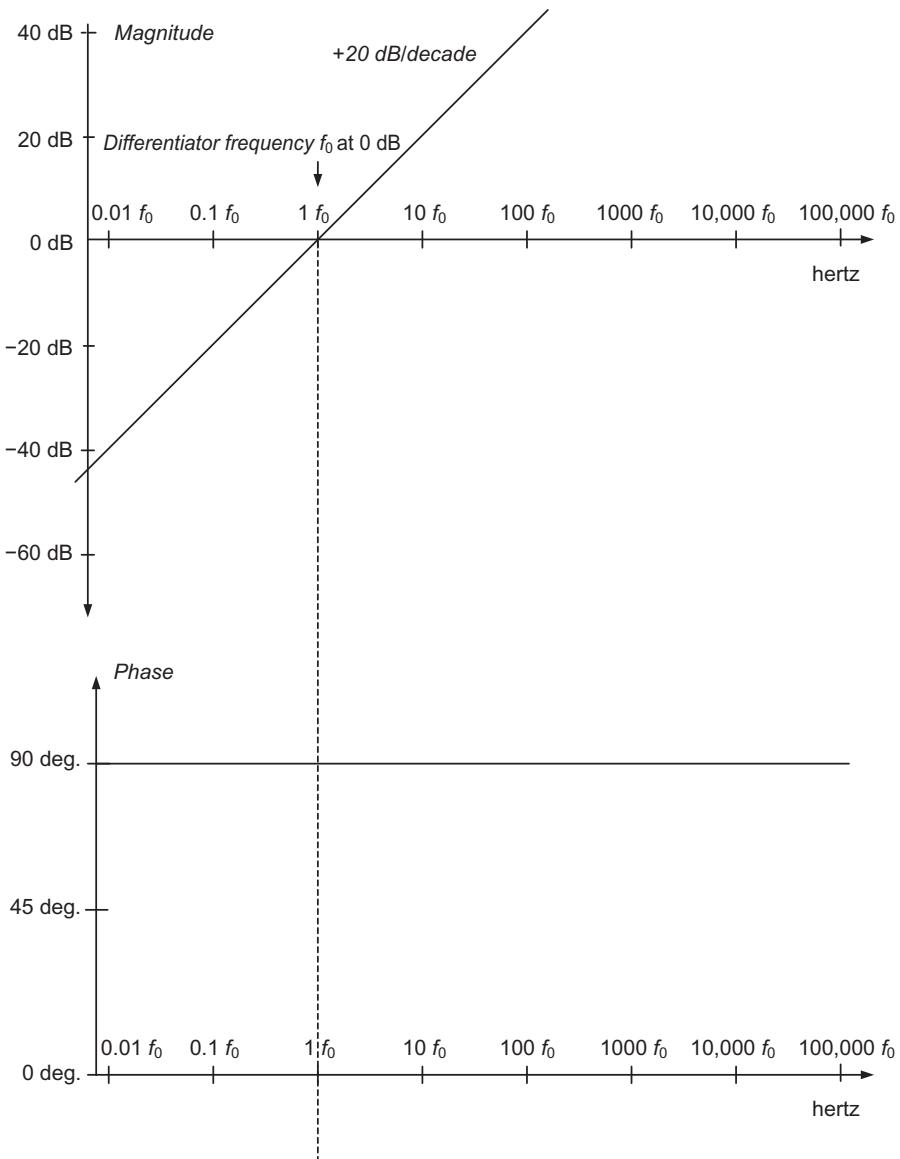


**Figure 5.19**   Asymptotic Bode plots of a pure differentiator.

Figure 4.10. The op amp-based differentiator has a negative infinite gain at DC. The gain or magnitude increases at a constant rate of 20 dB per decade of frequency. The first-order *RC* HPF differentiator circuit (Chapter 4, Fig. 4.10), which has no op amp, has a negative gain that increases at 20 dB per frequency decade from very low frequencies up until the filter cutoff frequency. Above this frequency, the op amp-less differentiator gain is 0 dB. Refer to the previously discussed circuit in Chapter 4, Figures 4.10 and 4.12. So what does this all mean in terms of practical operation of the differentiator? The op amp-based differentiator of Figure 5.18 actually will not work properly. Why? Because the gain at higher frequencies becomes extremely large; in fact, this high frequency gain is so large that any noisy or unwanted signals of a frequency higher than that of the signal that we intend to differentiate overwhelms the output of the op amp, effectively saturating it, and the op amp may even oscillate from rail to rail. To make the circuit of Figure 5.18 work, one has to limit the gain of the differentiator at very high frequencies. The implementation of such circuit, which will be used as a practical differentiator as well as an integrator, is discussed in the next section.

### 5.4.8  A Practical Integrator and Differentiator Circuit

We already discussed the reasons why the integrator circuit of Figure 5.16 and the differentiator circuit of Figure 5.18 will not operate properly. We summarize those results again. The integrator has an infinite gain at DC and thus it saturates the op amp output when a DC level is integrated for some finite time. The differentiator has an infinite gain for infinitely high frequencies, thus causing any high frequency unwanted signals to saturate the op amp and masking the differentiated signals of interest.

A practical solution to mitigate both of those problems is to limit the gain of the integrator at low frequencies and to limit the gain of the differentiator at very large frequencies. The circuit that does just that is depicted in Figure 5.20. Its corresponding asymptotic and exact Bode plots are presented in Figures 5.21 and 5.22, respectively.

The circuit in Figure 5.20 shapes the gain characteristics at low frequencies and at high frequencies. Refer once more to Figures 5.21 and 5.22. These figures show a fairly constant band-pass gain characteristic of 20 dB between cutoff frequencies $f_2$ and $f_3$. It behaves as a differentiator for all those signals of frequencies at $f_1$ and below, and it behaves as an integrator for those frequencies at $f_4$ and above. The cut-off frequencies are the –3 dB gain frequencies, for this particular example $f_2 = 100\,\text{Hz}$ and $f_3 = 10\,\text{kHz}$. Frequency range $f_2$ through $f_3$ defines the circuit mid-frequency band.

In other words our circuit combines the differentiating and integrating characteristics of both pure differentiator and pure integrator, and provides a flat gain band-pass characteristic at mid frequencies. Frequencies below $f_1$ are attenuated at a rate of +20 dB/decade. Frequencies above $f_4$ are attenuated at
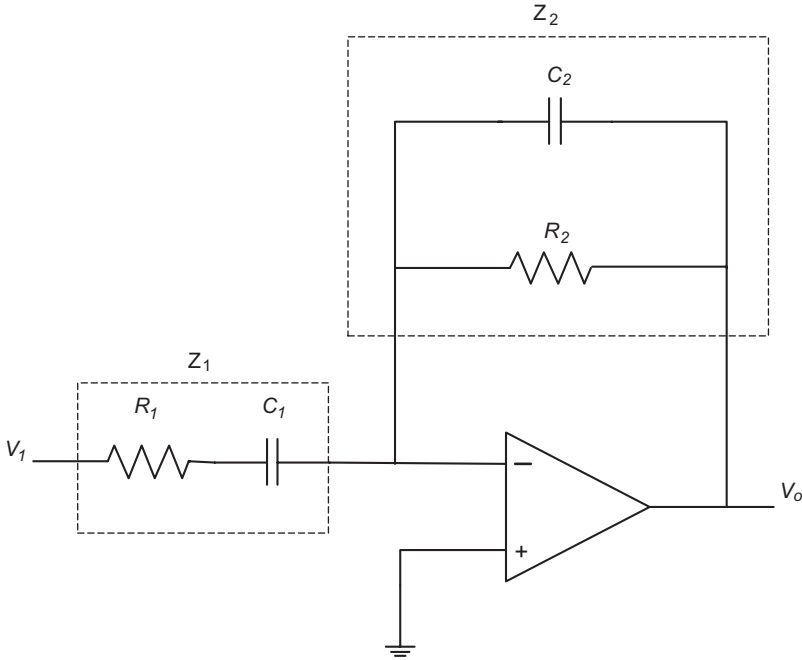
**Figure 5.20**   A practical differentiator, integrator, and band-pass filter circuit schematics.

a rate of $-20\,\text{dB/decade}$. At mid-band frequencies the gain is quite constant and it is $20\,\text{dB}$. Such gain is mainly determined by the ratio of $R_2$ over $R_1$.

In a general sense our practical circuit is designed such that at frequencies $f_2$ through $f_3$ the ratio of the impedance module of $R_2$ in parallel with $C_2$ over the impedance module of the series of $R_1$ and $C_1$ is 10, thus a $20\,\text{dB}$ gain. Capacitor $C_1$ and resistor $R_2$ determine $f_1$ at $0\,\text{dB}$ gain, the high end of the differentiating frequency range. $C_2$ and $R_1$ determine $f_4$ at $0\,\text{dB}$, and it is the low end or the beginning of the integrating frequencies.

Our practical circuit phase behavior ranges from $-90°$ at low frequencies to $+90°$ at high frequencies. Now since the op amp produces a $-180°$ phase shift, the overall circuit phase spans from $-90°$ ($+90°$ to $180°$) from very low frequencies down to $-270°$ ($-90°$ to $180°$) at high frequencies. The $-180°$ phase shift is caused by the negative sign of the op amp-based inverting configuration output voltage over input voltage transfer function, that is, $V_o/V_{in} = -R_2/R_1$.

We can see that the topology of the circuit of Figure 5.20 is that of an inverting amplifier where

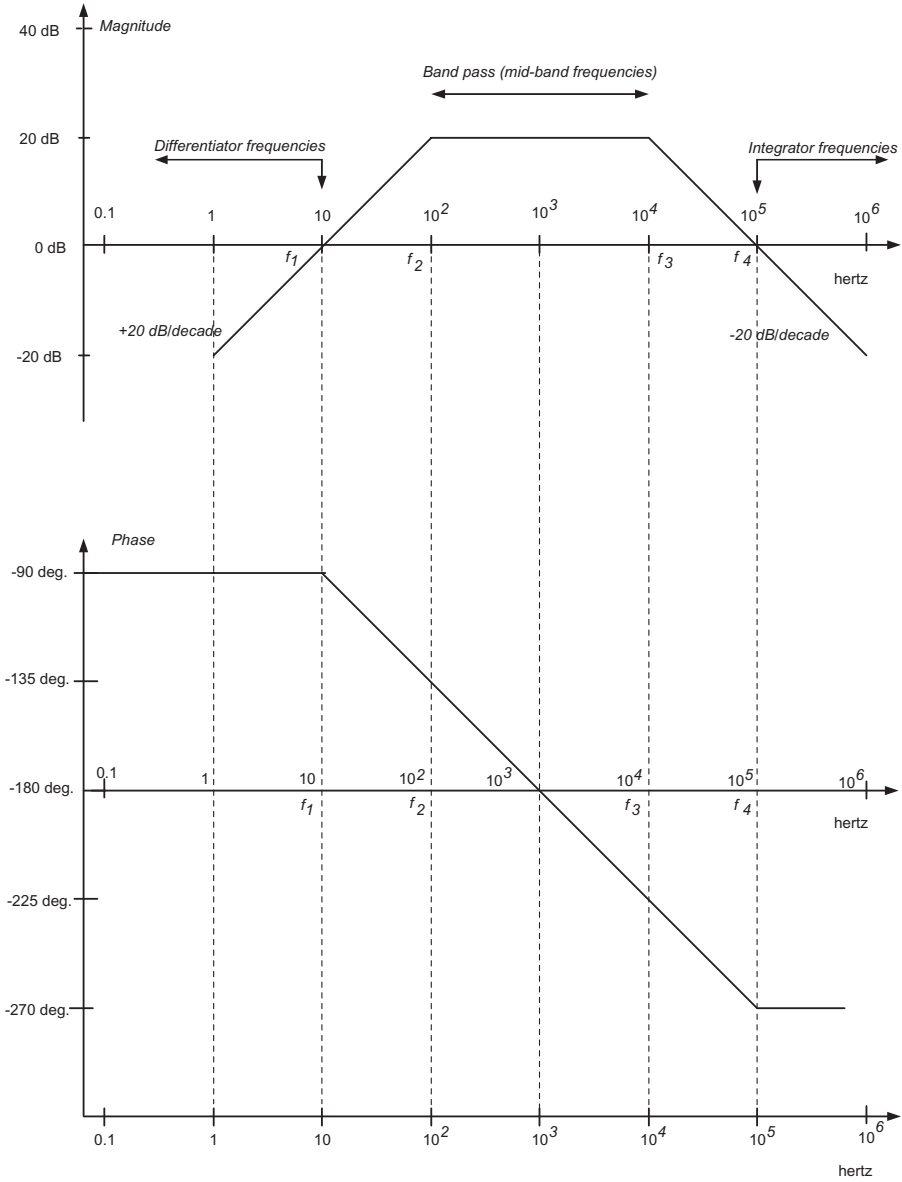$$Z_2 = \frac{1}{\dfrac{1}{R_2} + j\omega C_2} \tag{5.80}$$

**Figure 5.21**    Asymptotic Bode plots of a practical differentiator, integrator, and band-pass filter.
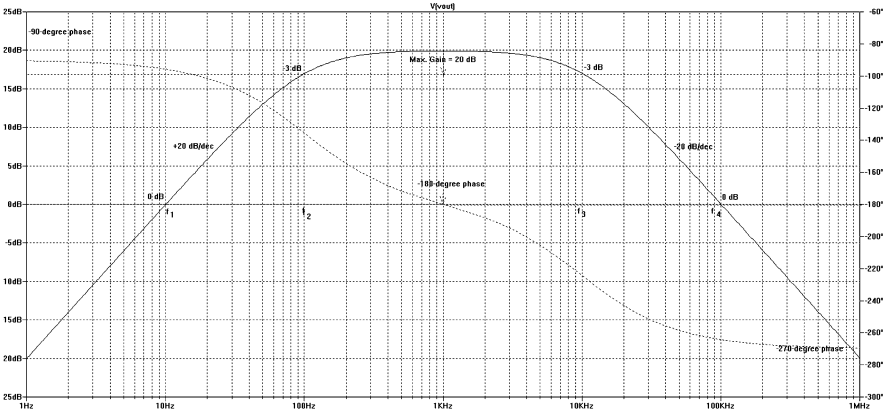
**Figure 5.22**   Exact Bode plots of a practical differentiator, integrator, and band-pass filter. See the Appendix to this chapter for a larger version.

and

$$Z_1 = R_1 + \frac{1}{j\omega C_1}. \tag{5.81}$$

The transfer function of the circuit of Figure 5.20 is

$$\frac{V_o}{V_1} = -\frac{Z_2}{Z_1}. \tag{5.82}$$

Using Equations (5.80) and (5.81) in Equation (5.82) we obtain

$$\frac{V_{out}}{V_{in}} = -\frac{\dfrac{1}{\dfrac{1}{R_2} + j\omega C_2}}{R_1 + \dfrac{1}{j\omega C_1}}. \tag{5.83}$$

Doing some algebraic manipulations with Equation (5.83) we arrive at

$$V_o / V_{in} = -\frac{j\omega R_2 C_1}{(1 + j\omega R_2 C_2)(1 + j\omega R_1 C_1)}. \tag{5.84}$$

Equation (5.84) has one zero at the origin in the numerator and two zeros on the denominator. Numerator zeros are simply referred to as zeros of the transfer function. Denominator zeros are referred to as poles of the transfer function.

We can rewrite Equation (5.84) using the following definitions:

$$\omega_1 = \frac{1}{R_2 C_1} \tag{5.85}$$

$$\omega_2 = \frac{1}{R_1 C_1} \tag{5.86}$$

$$\omega_3 = \frac{1}{R_2 C_2} \text{ and } \omega_4 = \frac{1}{R_1 C_2} \tag{5.87}$$

where $\omega_1 = 2\pi f_1$, $\omega_2 = 2\pi f_2$, $\omega_3 = 2\pi f_3$, and $\omega_4 = 2\pi f_4$ thus,

$$f_1 = 1/2\pi R_2 C_1 \tag{5.88}$$

$$f_2 = 1/2\pi R_1 C_1 \tag{5.89}$$

$$f_3 = 1/2\pi R_2 C_2 \text{ and } f_4 = 1/2\pi R_1 C_2 \tag{5.90}$$

We can plot Equation (5.84) either by writing a computer program that calculates the magnitude and the phase of Equation (5.84) or using the asymptotic Bode plot methodology. We have to keep in mind that Equation (5.88) is the frequency at which the transfer function magnitude has 0 dB gain and the differentiation in the time domain ends. Equation (5.89) is where the first pole of the transfer function is placed, and $f_3$ (in Eq. ((5.90))) is where the second pole of the transfer function is placed. Finally, $f_4$ is the frequency at which the gain is 0 dB and integration begins.

We will go over a numerical example to clarify the generation of the transfer function given by Equation (5.84).

**Example 5.8**  Design a pass band amplifier that has the following characteristics:

(a)  Pass band gain = 20 dB
(b)  0 dB gain and end of differentiation at $f_1$ = 10 Hz
(c)  Low cutoff frequency $f_2$ = 100 Hz
(d)  High cut-off frequency $f_3$ = 10 kHz
(e)  0 dB gain and beginning of integration at 100 kHz

Assume you can use an ideal op amp.

The circuit topology is just like the circuit shown in Figure 5.20.

From Equations (5.88)–(5.90) and the given characteristics of the desired band pass amplifier with combined differentiating and integrating properties, we have the following:

$$f_1 = 1/2\pi R_2 C_1 = 10 \text{ Hz} \tag{5.91}$$

$$f_2 = 1/2\pi R_1 C_1 = 100 \text{ Hz} \tag{5.92}$$

$$f_3 = 1/2\pi R_2 C_2 = 10 \text{ kHz and } f_4 = 1/2\pi R_1 C_2 = 100 \text{ kHz.} \tag{5.93}$$

The mid-band frequency gain of our amplifier has to be 20 dB. This means that the amplifier closed loop gain has to be 10. Arbitrarily, we can choose $R_2 = 10$ kΩ, thus $R_1$ must be $1$ kΩ, thus $20 \log_{10} (10) = 20$ dB. Using these values for $R_1$ and $R_2$ in Equations (5.91)–(5.93) we obtain

$$C_1 = 1.59 \ \mu F \tag{5.94}$$

$$C_2 = 1.59 \ \text{nF}. \tag{5.95}$$

Also remember that

$$R_1 = 1 \ \text{k}\Omega \tag{5.96}$$

and

$$R_2 = 10 \ \text{k}\Omega. \tag{5.97}$$

Figure 5.22 shows exact Bode magnitude and phase plots of the transfer function given by Equation (5.84) using the numerical values given by Equations (5.94) through (5.97).

> ***Important Points***
> *The differentiating frequencies of the amplifier are at and below $f_1$ (10 Hz and below).*
> *The band pass flat gain of 20 dB is between $f_2 = 100$ Hz and $f_3 = 10$ kHz.*
> *The integrating frequencies of the amplifier are at and above $f_4$ (100 kHz and above).*
> *The current circuit topology will work as a differentiator, a band pass amplifier, and an integrator in the three different frequency ranges discussed above (see Figs. 5.21 and 5.22).*

## 5.5   OP AMPS NONLINEAR APPLICATIONS

The most significant and widely used nonlinear application using op amps is when op amps operate in open loop. The op amp under such operation is referred to as a comparator, and op amp manufacturers optimize op amp parameters to operate them as comparators. So it is common for IC manufacturers to sell op amps and comparators. So what is a comparator? A comparator is designed to operate in open loop; its output swings between specified upper and lower limits. A very desirable feature is that the comparator wants to be fast to swing its output upon a detected voltage difference at its inputs. Usually comparators do not have internal compensating capacitors. On the other hand, op amps have internal compensating capacitors. The lack of compensation capacitors allows comparators to be faster than op amps. Op amps are designed to be accurate and stable; op amps have good DC and AC behavior. On a final note, most comparators have an open collector or open drain

output; this means that its output can be connected to supply levels that may not necessarily be those of the comparator power supplies. This flexibility allows an easier interface of comparators to digital circuits.

### 5.5.1   The Open-Loop Comparator

The comparator is typically used in open-loop mode to compare when the signal level at the one of the inputs is greater or smaller that the signal level at the other input terminal. Since a comparator gain is very high, just like that of an open-loop op amp, upon detecting a difference between its inputs, the output will swing to the positive rail when V+ > V−. The output will swing to the negative rail when V− > V+. V+ refers to the input signal at the noninverting input of the comparator. V− is the signal at the inverting input of the comparator. Figure 5.23 shows a comparator operating with its inverting input tied to ground and an arbitrary waveform at its noninverting input. Note that when the input signal at the positive input is above zero the comparator output swings to its positive rail.

The output swings to the negative rail when the noninverting input signal is negative or below ground.

Figure 5.23 assumes that the comparator output used is very fast when reacting to a change of the noninverting input. Such circuit is called a noninverting zero-crossing detector. Note that since the inverting input of the comparator is grounded, it is at 0 V; every time the noninverting input is above zero, the output of the comparator saturates toward the positive rail, otherwise it saturates to the negative rail. We can easily design an inverting zero-crossing detector by swapping the inputs to the comparator of Figure 5.23. This means tying the ground to the noninverting input and connecting the input signal $V_{in}$ to the inverting input.

### 5.5.2   Positive and Negative Voltage-Level Detectors Using Comparators

#### 5.5.2.1   *Positive Level Detectors*   Let us assume that we want to detect when a signal $V_{in}$ is above a positive DC voltage level, which we will refer to as $V_{REF}$. Let us also assume that every time signal $V_{in}$ is above $V_{REF}$, we want the output of the comparator to indicate this with a high output level at $V_{out}$. Figure 5.24 shows a possible implementation of such circuit.

Note that the reference voltage $V_{REF}$ is connected to the inverting input of the comparator. The input signal $V_{in}$ is tied to the noninverting input of the comparator. The comparator shows its positive and negative power supply levels. For simplicity, the decoupling capacitors are not shown. Let us see how this circuit works; each time $V_{in}$ is greater than $V_{REF}$, the comparator output will saturate to the positive $+V_{SAT}$ level. When $V_{in}$ is less than $V_{REF}$ the comparator output will saturate at the negative $-V_{SAT}$ level. Although Figure 5.24 shows a sinusoidal waveform for $V_{in}$, there is no restriction on waveform $V_{in}$,
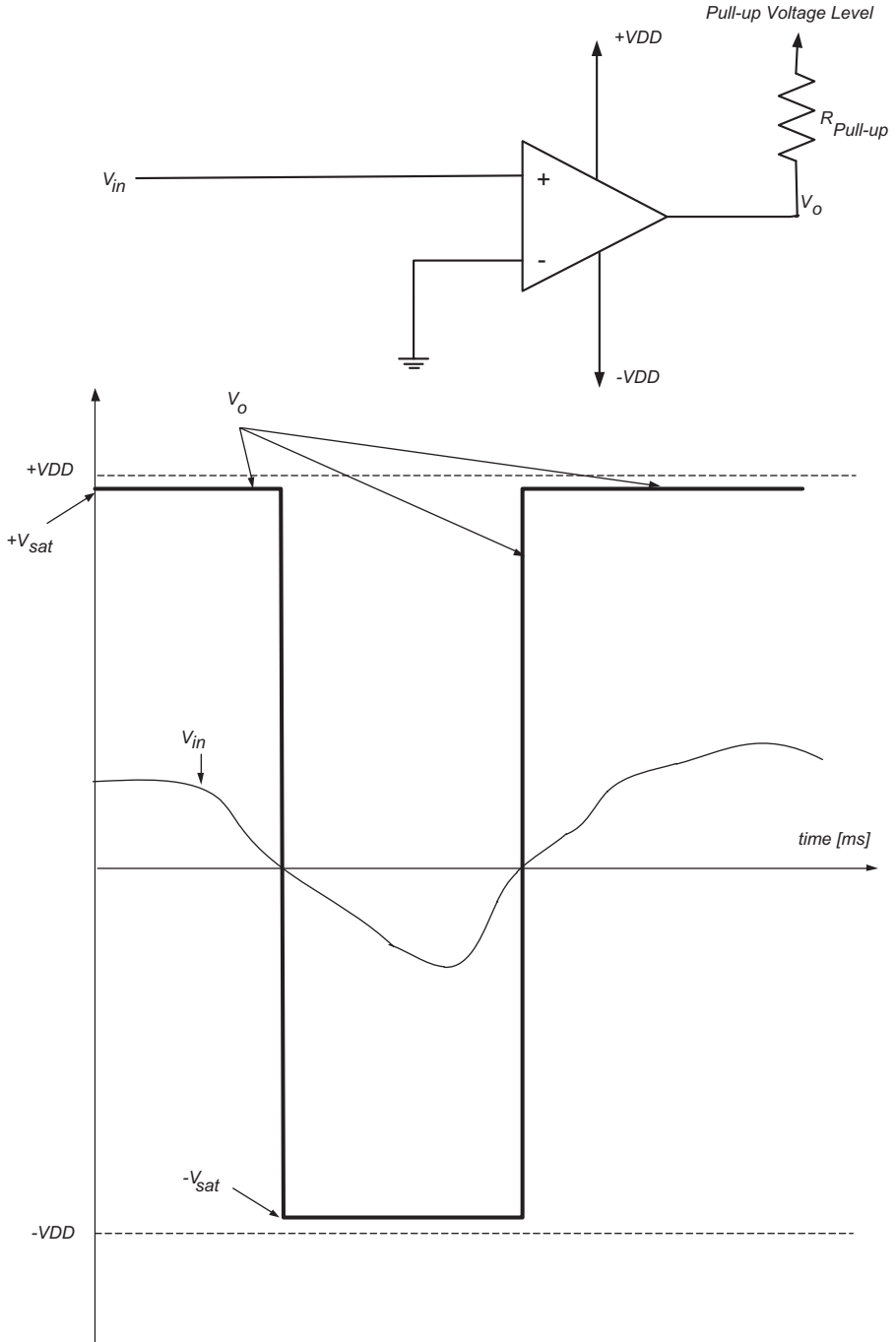
**Figure 5.23** Open-loop comparator operation with grounded inverting input.
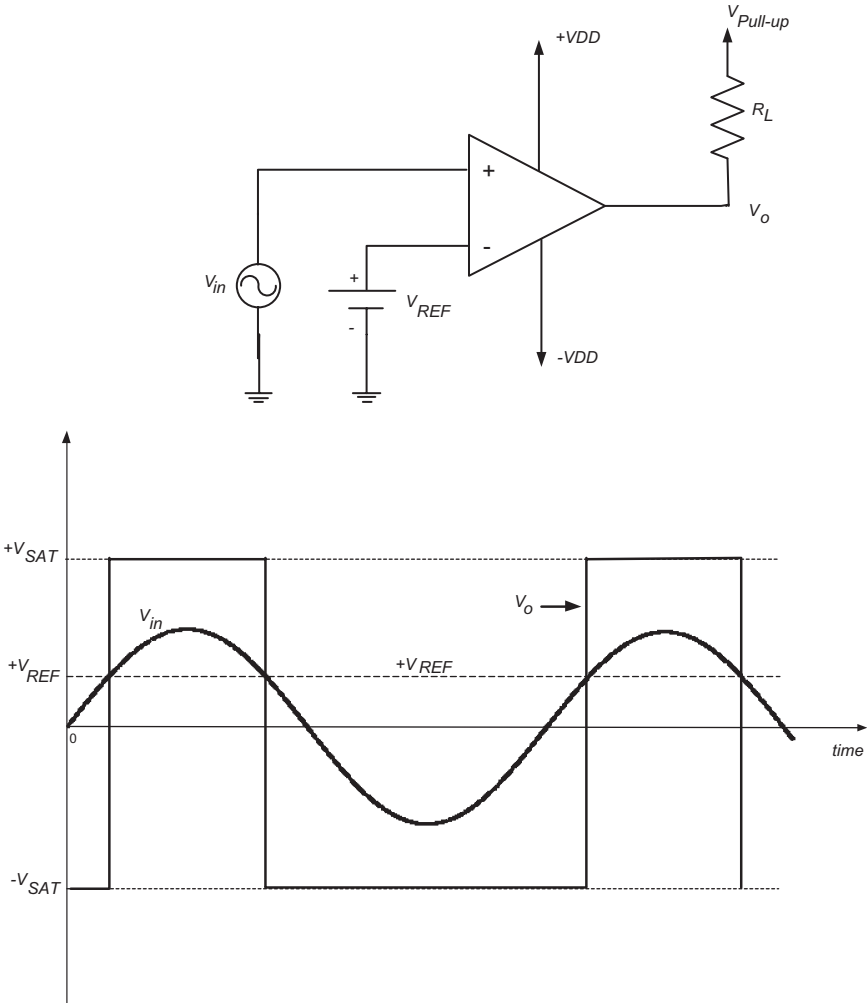
**Figure 5.24**   Noninverting positive-level detector.

it can be a saw-tooth, an exponential or even a piece-wise linear waveform. The positive-level detector of Figure 5.24 is referred to as a noninverting detector because the comparator output signals with a high level $V_{out}$ at $+V_{SAT}$ when the input signal $V_{in}$ is greater than the reference voltage. This is the simplest and most straightforward variation of the four types of level detectors that we will study in this section. When confused with the subsequent detector, make sure that you always come back to the one described by Figure 5.24. This will let one understand the concepts more easily than any of the other three will. The inverting positive-level detector is implemented in Figure 5.25. Note that the input signal is now applied to the inverting input of the comparator, while the reference voltage is applied to the noninverting input.
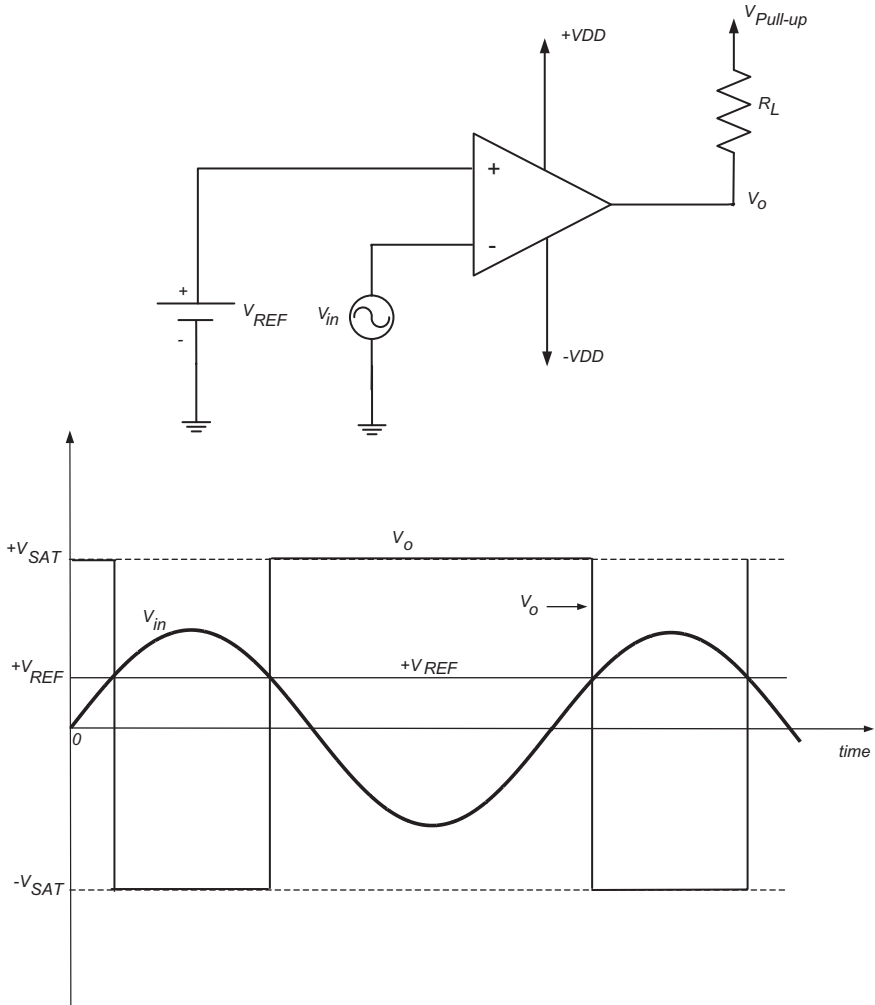
**Figure 5.25**    Inverting positive-level detector.

**5.5.2.2 Negative-Level Detectors**    Just like there are two polarities of positive-level detectors, that is, inverting and noninverting, there are also two kinds of negative-level detectors. Negative level refers to the sign of the voltage, to which the input signal is being compared. Figure 5.26 depicts a noninverting negative-level voltage detector. $V_{in}$ the input signal is applied to the positive input of the comparator, while the negative input of the comparator has a negative reference voltage. Note that $V_{REF}$ negative terminal is connected to the comparator inverting input, while the positive terminal of $V_{REF}$ is grounded.

Finally, for the inverting level negative edge voltage level detector, $V_{REF}$ and $V_{in}$ are swapped. Figure 5.27 depicts the inverting negative voltage-level detector. Note that when $V_{in}$ is above the negative reference level ($-V_{REF}$), the output of the comparator is at $-V_{SAT}$.
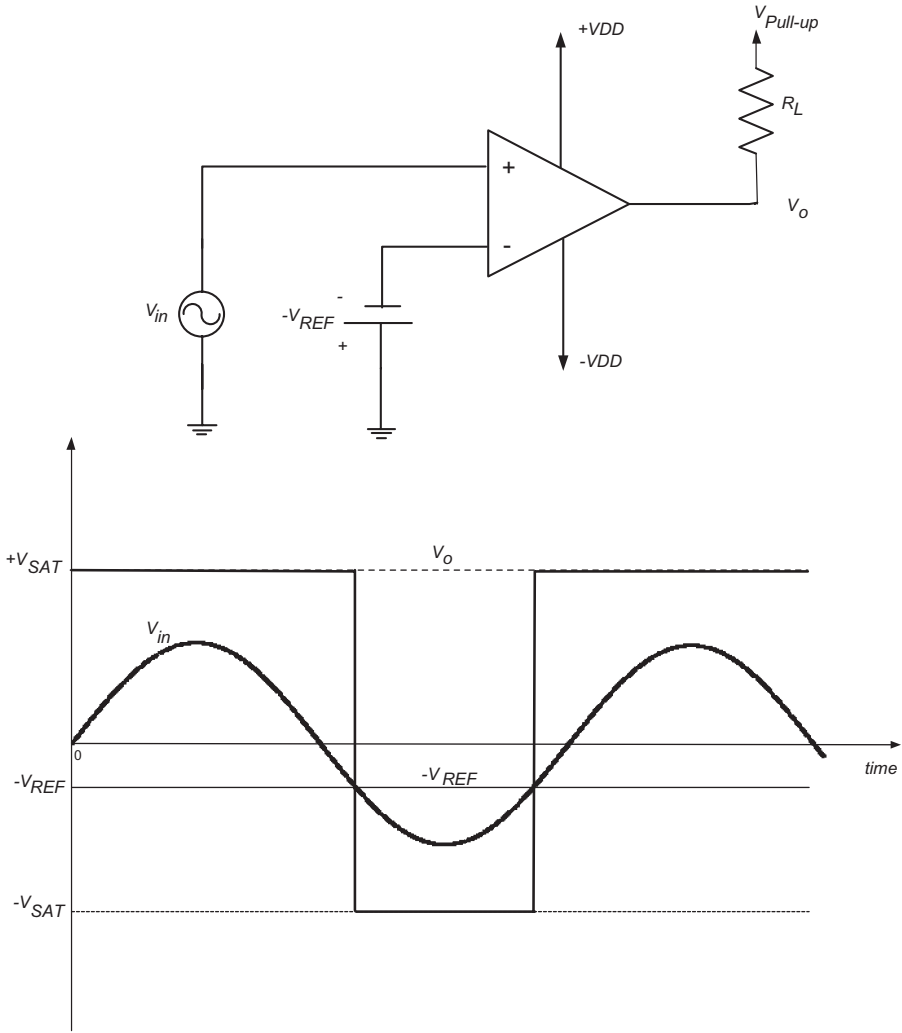
**Figure 5.26** Noninverting negative voltage-level detector.

*Summary of Voltage Level Detectors:*

1. Noninverting positive-level detector (see Fig. 5.24)
2. Inverting positive-level detector (see Fig. 5.25)
3. Noninverting negative-level detector (see Fig. 5.26)
4. Inverting negative-level detector (see Fig. 5.27)

### 5.5.3 Comparator with Positive Feedback (Hysteresis)

Comparators work well in open-loop mode if the signal $V_{in}$ at its input varies rapidly and it is not noisy. However, if a noisy input signal $V_{in}$ is present, there is
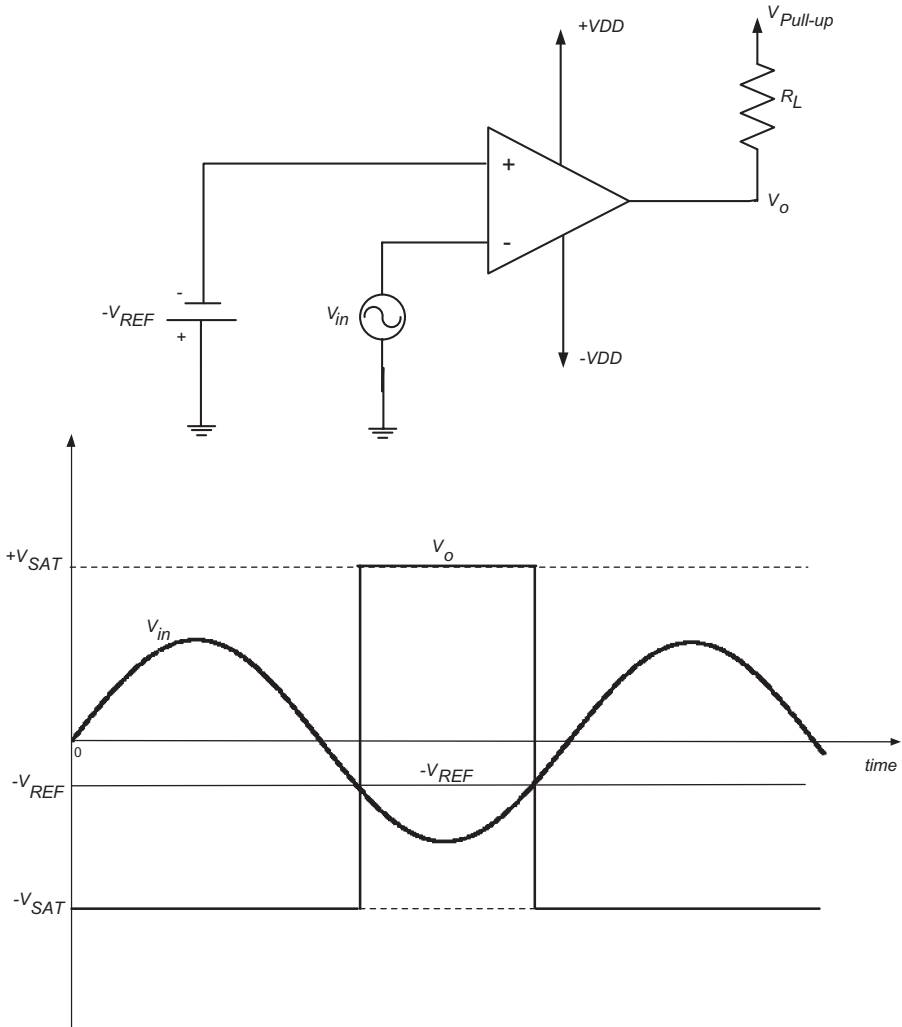
**Figure 5.27**    Inverting negative voltage-level detector.

a good opportunity for the open-loop comparator to oscillate once or more times before settling on its steady state either $+V_{SAT}$ or $-V_{SAT}$ output voltage level. Figure 5.28 shows a comparator operating in open-loop; the input signal has on top of it a noisy signal of much higher frequency than the input. We can observe that before the output settles to its final and correct value, the comparator output oscillates momentarily; this is referred to as *chattering*. A straightforward way of significantly reducing or eliminating this problem is to provide a little bit of positive feedback from the comparator output back into its positive input.

Taking a fraction of the output voltage and feeding it back to the noninverting input of the comparator provides positive feedback into the comparator.
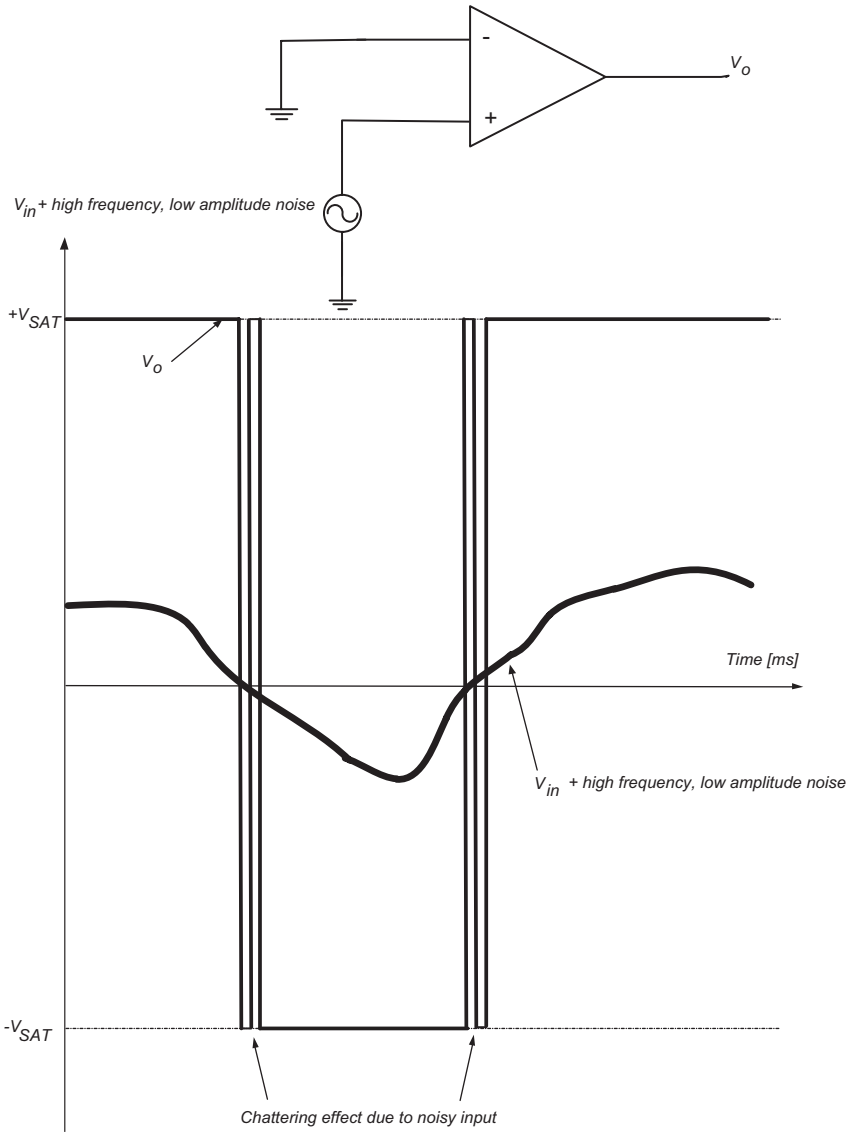
**Figure 5.28** Comparator operating in open-loop mode that exhibits chattering.

Figure 5.29 shows a comparator with resistors $R_1$ and $R_2$ that provide positive feedback. The circuit is configured as a noninverting zero voltage-level detector. Let us understand how the resistors provide hysteresis to the circuit.

The upper threshold voltage is the output voltage times the resistor divider formed by $R_1$ and $R_2$. Thus,

$$V_{UT} = \frac{R_2}{R_1 + R_2} V_{SAT}. \tag{5.98}$$
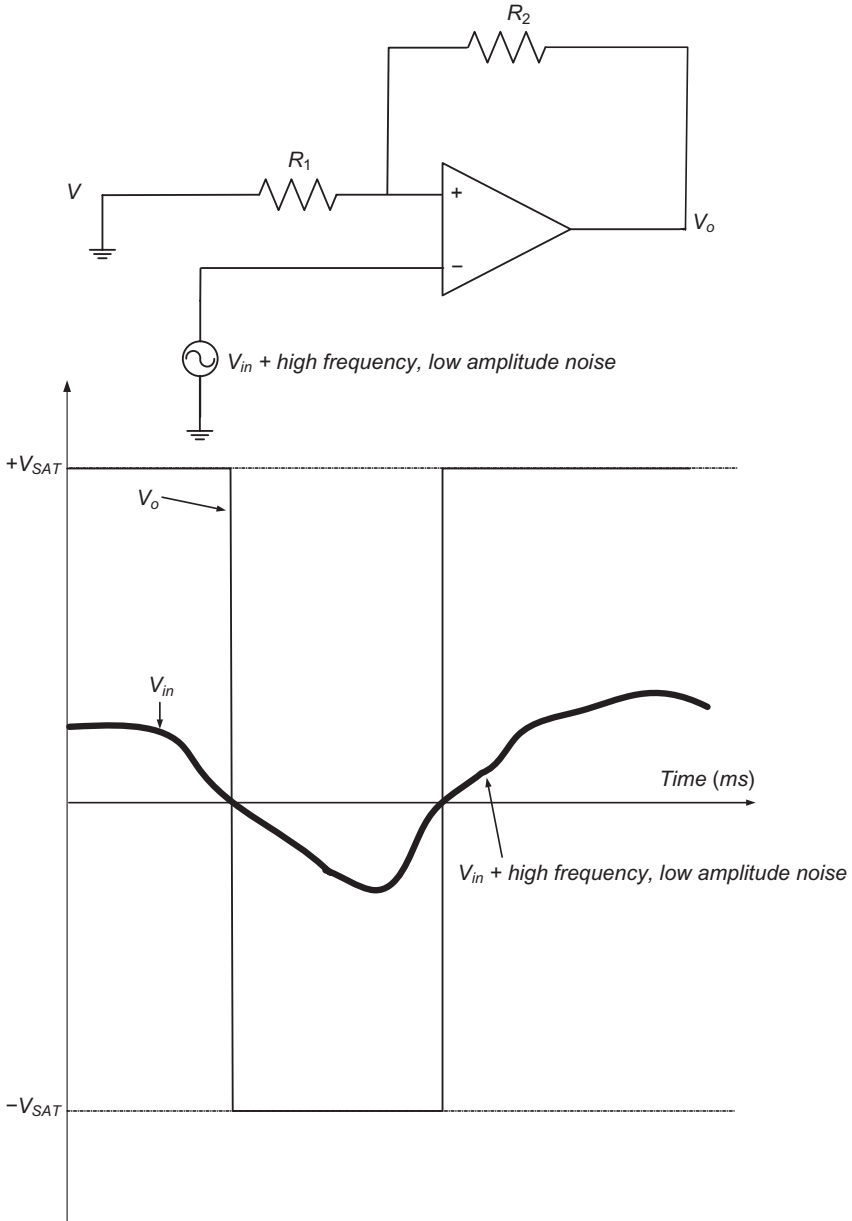
**Figure 5.29** Comparator with hysteresis eliminates chattering.

When the comparator output voltage is equal to $+V_{SAT}$ the upper threshold voltage given by Equation (5.98) is a fraction of $V_{SAT}$. If $V_{in}$ plus any noisy and unwanted components are present and are in absolute magnitude smaller that $V_{UT}$, the comparator snaps to $+V_{SAT}$ and will get locked at $+V_{SAT}$. As $V_{in}$ decreases below 0 V (the ground level) $+V_{SAT}$ will eventually snap out of $+V_{SAT}$

and will switch to $-V_{SAT}$. Now $-V_{SAT}$ produces a voltage called the lower threshold, which is equal to

$$V_{LT} = -\frac{R_2}{R_1 + R_2} V_{SAT}. \tag{5.99}$$

The noise on top of $V_{in}$ is still smaller in magnitude that the $V_{LT}$. The comparator output locks up at $-V_{SAT}$ now. As the input continues to decrease well below ground, the output of the comparator stays at $-V_{SAT}$. Not until $V_{in}$ grows above ground the whole cycle repeats itself indefinitely. Every time the comparator output locked up to either $+V_{SAT}$ or $-V_{SAT}$, the undesirable chattering seen in the open-loop case of the previous section has been eliminated. Figure 5.29 shows a comparator with hysteresis.

**Example 5.9**   Given a 100 Hz triangular waveform, and assuming that noise signals of ±10 mV can be riding on the signal, design the hysteresis circuit divider to avoid chattering of the combined signal plus noise on a noninverting zero voltage detector. Let us assume that the positive and negative supplies of the comparator are respectively + and –15 V. Also assume that you checked the comparator data sheet and the + and $-V_{SAT}$ voltages are respectively + and –14 V.

Choosing $R_2 = 100\ k\Omega$ and $R_1 = 100\ \Omega$, using these values in Equations (5.98) and (5.99) we find that

$$V_{UT} = \frac{R_2}{R_1 + R_2} V_{SAT} = \frac{100k\Omega}{100k\Omega + 100\Omega} 14\ \text{V} \cong 14\ \text{mV} \tag{5.100}$$

and

$$V_{LT} = -\frac{R_2}{R_1 + R_2} V_{SAT} = -\frac{100k\Omega}{100k\Omega + 100\Omega} 14\ \text{V} \cong -14\ \text{mV}. \tag{5.101}$$

The total hysteresis voltage, or the voltage range for which the error on the signal is eliminated, is given by

$$V_H = V_{UT} - V_{LT} = 28\ \text{mV}. \tag{5.102}$$

Note that when the input signal goes above the upper threshold, the output voltage drops down to $-V_{SAT}$. The peak-to-peak noise voltage on the input signal has to be greater than or equal to 28 mV (the hysteresis voltage given by Equation (5.102)), to pull the input signal below the lower threshold and cause a false zero crossing. So as long as the peak-to-peak noise on top of the input signal does not exceed the hysteresis voltage range ($V_H$), the false crossing will not occur. Since for this example we are told that the peak-to-peak

noise can be up to 20 mV and since the comparator hysteresis was designed to tolerate 28 mV of peak-to-peak noise, we still have a positive margin over the required immunity to noise.

## 5.6   OPERATIONAL AMPLIFIERS NONIDEALITIES

The actual electrical characteristics of real op amps are more complicated than those of the idealized op amp. The op amp is implemented with either bipolar or JFET transistors. The basic op amp consists of three main stages cascaded one after the other. The input stage is a transistorized differential stage, a level shifting stage follows the first stage and the last stage is an output stage that performs a differential to single ended output conversion. Differential signals come in pairs; there is a noninverted signal and an inverted signal to carry information over two separate wires. This provides to the signal better noise immunity; this is to say that the signals are more protected against noise or unwanted signals. Single ended signals are referenced with respect to ground and do not have as good noise immunity as differential signals do.

The differential input stage of the op amp has imperfections due to the fact that it is impossible to fabricate perfectly matched transistors. The currents in or out of the inverting and noninverting inputs are not really zero. They are nonzero and but small in magnitude, and they are referred to as the bias currents. There is an $I_{B+}$ (positive input bias current) and an $I_{B-}$ (negative input bias current). We will model this behavior of the input stage of the op amp with to current sources of values $I_{B+}$ and $I_{B-}$. Figure 5.30 shows the model of a real op amp with the imperfections that we describe throughout this entire section. It is important to say that such bias currents are not only nonzero, but also they are not equal to each other and may flow in or out of their respective op amp input. The magnitude of the difference of the positive and negative bias current is referred to as the offset current ($I_{OS}$). The numerical value of the offset current generally is a fraction of the bias current. A voltage source models the offset voltage of the amplifier. The offset voltage ($V_{OS}$) of the op amp is the voltage that is required to apply across its inputs to obtain a 0 V output with the op amp in an open-loop condition. Differential impedance appears across both op amp inputs and common mode impedance appears between the inputs and ground. This impedance models the finite common mode the real op amp has. Figure 5.30 depicts an op amp model with some real electrical parameters.

The input stage has two AC current sources ($I_N$) and an AC voltage source ($V_N$) that model noise components that unavoidably exist in the op amp. Finally, for the input imperfections, we have to mention that both bias currents and offset voltages vary or drift with temperature variations. Manufacturers usually specify these parameters at one temperature, for example, at 25°C and at a range of temperatures, such as –40°C to 85°C.

Let us now talk about the output stage of the real op amp. The output of the op amp has a nonzero and finite output resistance ($R_o$), which is modeled
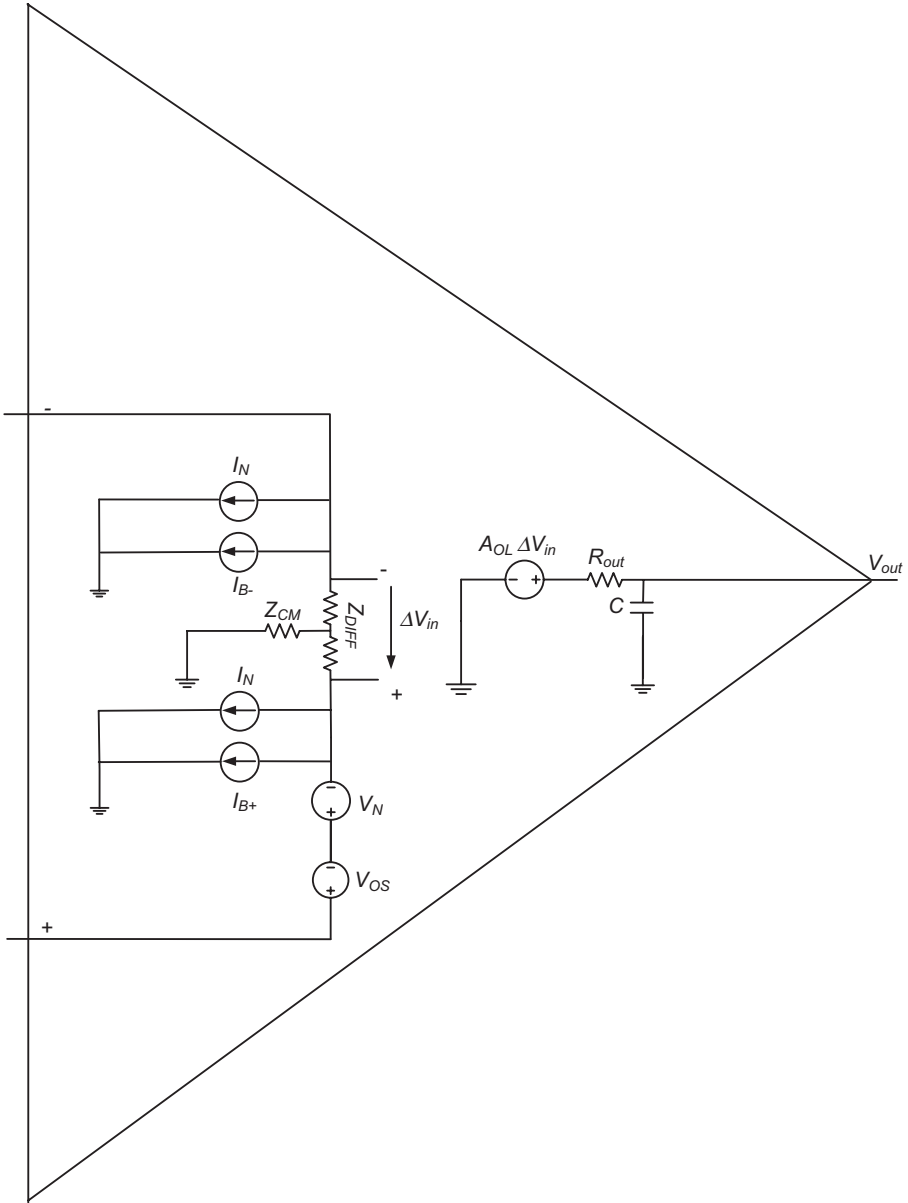
**Figure 5.30** Model of a real operational amplifier.

in series with the output generator $A_{OL}$ (Fig. 5.30). Generator $A_{OL}$ models the finite nature of the op amp open-loop gain. In actuality $A_{OL}$ is really large, but it is not infinite. The op amp open-loop gain is also a function of frequency, and it is usually modeled with a capacitor hanging from the output of the op amp to ground. This $RC$ network at the output of the op amp is also referred to as the op amp single pole approximation. The op amp manufacturer specifies the device behavior with frequency with the open-loop gain bandwidth and with the op amp gain-bandwidth product. Both of these parameters model the frequency behavior of the op amp under small signal excitation. A small signal for an op amp is a signal whose amplitude is about one order of magnitude smaller that its supply voltage. For large signal operation, the slew-rate of the op amp determines how fast the op amp can react to changes. Slew is usually specified in volts per microsecond. A slow op amp may have a 0.5 V/µs slew-rate, while a high speed one may have a 6000 V/µs slew-rate.

There are a few more real parameters of an op amp such as common mode rejection ratio (CMRR), which provides information as to how much common mode signals become attenuated, by the op amp. CMRR is also a frequency-dependent parameter. Power supply rejection ratio specifies how sensitive the op amp operation is to variation of it power supply rails. This section intends to cover some of the most fundament imperfections that most op amp manufacturers specify. Beware that this list is not complete and there are manufacturers that provide more or less complete data sheet specifications for their devices. Table 5.7 summarizes some commonly specified op-amp parameters.

## 5.7  OP AMP SELECTION CRITERIA

Op amps are generally classified by the following characteristics:

1. DC parameters (offset voltage, bias and offset currents, and their drift with temperature) as precision op amps,
2. Low noise,
3. Speed (gain-bandwidth product and slew-rate),
4. Single or dual rail power supply,
5. Single, dual, or quad (1, 2, or 4 amplifiers) in a package,
6. Rail-to-rail output voltage swing,
7. Maximum common mode input voltage, low power consumption. Ultimately most manufacturers provide online tools to their customers to select any of their op amps by a selection of any number and combination of parameters offered by the manufacturer. Other characterizations exist; just a few of the most popular ones were listed above.

Why can't we have all of the parameters optimized and not worry about selecting op amps? The reason is that improving some op amp parameters imposes

**Table 5.7    Real op amp parameters (National LM741, reproduced with permission of Texas Instruments Incorporated)**

LM741

## Absolute Maximum Ratings (Note 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**
(Note 7)

|  | LM741A | LM741 | LM741C |
|---|---|---|---|
| Supply Voltage | ±22V | ±22V | ±18V |
| Power Dissipation (Note 3) | 500 mW | 500 mW | 500 mW |
| Differential Input Voltage | ±30V | ±30V | ±30V |
| Input Voltage (Note 4) | ±15V | ±15V | ±15V |
| Output Short Circuit Duration | Continuous | Continuous | Continuous |
| Operating Temperature Range | −55˚C to +125˚C | −55˚C to +125˚C | 0˚C to +70˚C |
| Storage Temperature Range | −65˚C to +150˚C | −65˚C to +150˚C | −65˚C to +150˚C |
| Junction Temperature | 150˚C | 150˚C | 100˚C |
| Soldering Information |  |  |  |
| N-Package (10 seconds) | 260˚C | 260˚C | 260˚C |
| J- or H-Package (10 seconds) | 300˚C | 300˚C | 300˚C |
| M-Package |  |  |  |
| Vapor Phase (60 seconds) | 215˚C | 215˚C | 215˚C |
| Infrared (15 seconds) | 215˚C | 215˚C | 215˚C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering

surface mount devices.

|  | | | |
|---|---|---|---|
| ESD Tolerance (Note 8) | 400V | 400V | 400V |

## Electrical Characteristics (Note 5)

| Parameter | Conditions | LM741A Min | LM741A Typ | LM741A Max | LM741 Min | LM741 Typ | LM741 Max | LM741C Min | LM741C Typ | LM741C Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $T_A$ = 25˚C |  |  |  |  |  |  |  |  |  |  |
|  | $R_S \leq$ 10 kΩ |  |  |  | 1.0 | 5.0 |  | 2.0 | 6.0 | | mV |
|  | $R_S \leq$ 50Ω |  | 0.8 | 3.0 |  |  |  |  |  | | mV |
|  | $T_{AMIN} \leq T_A \leq T_{AMAX}$ |  |  |  |  |  |  |  |  | |  |
|  | $R_S \leq$ 50Ω |  |  | 4.0 |  |  |  |  |  | | mV |
|  | $R_S \leq$ 10 kΩ |  |  |  |  |  | 6.0 |  |  | 7.5 | mV |
| Average Input Offset Voltage Drift |  |  |  | 15 |  |  |  |  |  | | µV/˚C |
| Input Offset Voltage Adjustment Range | $T_A$ = 25˚C, $V_S$ = ±20V | ±10 |  |  | ±15 |  |  | ±15 |  | | mV |
| Input Offset Current | $T_A$ = 25˚C |  | 3.0 | 30 | 20 | 200 |  | 20 | 200 | | nA |
|  | $T_{AMIN} \leq T_A \leq T_{AMAX}$ |  |  | 70 | 85 | 500 |  |  | 300 | | nA |
| Average Input Offset Current Drift |  |  |  | 0.5 |  |  |  |  |  | | nA/˚C |
| Input Bias Current | $T_A$ = 25˚C |  | 30 | 80 | 80 | 500 |  | 80 | 500 | | nA |
|  | $T_{AMIN} \leq T_A \leq T_{AMAX}$ |  |  | 0.210 |  | 1.5 |  |  | 0.8 | | µA |
| Input Resistance | $T_A$ = 25˚C, $V_S$ = ±20V | 1.0 | 6.0 |  | 0.3 | 2.0 |  | 0.3 | 2.0 | | MΩ |
|  | $T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S$ = ±20V | 0.5 |  |  |  |  |  |  |  | | MΩ |
| Input Voltage Range | $T_A$ = 25˚C |  |  |  |  |  |  | ±12 | ±13 | | V |
|  | $T_{AMIN} \leq T_A \leq T_{AMAX}$ |  |  |  | ±12 | ±13 |  |  |  | | V |

**Table 5.7   (*Continued*)**

### Electrical Characteristics (Note 5)   (Continued)

| Parameter | Conditions | LM741A | | | LM741 | | | LM741C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Large Signal Voltage Gain | $T_A = 25°C$, $R_L \geq 2$ k$\Omega$ | | | | | | | | | | |
| | $V_S = \pm20V$, $V_O = \pm15V$ | 50 | | | | | | | | | V/mV |
| | $V_S = \pm15V$, $V_O = \pm10V$ | | | | 50 | 200 | | 20 | 200 | | V/mV |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$, | | | | | | | | | | |
| | $R_L \geq 2$ k$\Omega$, | | | | | | | | | | |
| | $V_S = \pm20V$, $V_O = \pm15V$ | 32 | | | | | | | | | V/mV |
| | $V_S = \pm15V$, $V_O = \pm10V$ | | | | 25 | | | 15 | | | V/mV |
| | $V_S = \pm5V$, $V_O = \pm2V$ | 10 | | | | | | | | | V/mV |
| Output Voltage Swing | $V_S = \pm20V$ | | | | | | | | | | |
| | $R_L \geq 10$ k$\Omega$ | $\pm16$ | | | | | | | | | V |
| | $R_L \geq 2$ k$\Omega$ | $\pm15$ | | | | | | | | | V |
| | $V_S = \pm15V$ | | | | | | | | | | |
| | $R_L \geq 10$ k$\Omega$ | | | | $\pm12$ | $\pm14$ | | $\pm12$ | $\pm14$ | | V |
| | $R_L \geq 2$ k$\Omega$ | | | | $\pm10$ | $\pm13$ | | $\pm10$ | $\pm13$ | | V |
| Output Short Circuit | $T_A = 25°C$ | 10 | 25 | 35 | | 25 | | | 25 | | mA |
| Current | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | 10 | | 40 | | | | | | | mA |
| Common-Mode | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | | | | | | | | |
| Rejection Ratio | $R_S \leq 10$ k$\Omega$, $V_{CM} = \pm12V$ | | | | 70 | 90 | | 70 | 90 | | dB |
| | $R_S \leq 50\Omega$, $V_{CM} = \pm12V$ | 80 | 95 | | | | | | | | dB |
| Supply Voltage Rejection | $T_{AMIN} \leq T_A \leq T_{AMAX}$, | | | | | | | | | | |
| Ratio | $V_S = \pm20V$ to $V_S = \pm5V$ | | | | | | | | | | |
| | $R_S \leq 50\Omega$ | 86 | 96 | | | | | | | | dB |
| | $R_S \leq 10$ k$\Omega$ | | | | 77 | 96 | | 77 | 96 | | dB |
| Transient Response | $T_A = 25°C$, Unity Gain | | | | | | | | | | |
| Rise Time | | | 0.25 | 0.8 | | 0.3 | | | 0.3 | | µs |
| Overshoot | | | 6.0 | 20 | | 5 | | | 5 | | % |
| Bandwidth (Note 6) | $T_A = 25°C$ | 0.437 | 1.5 | | | | | | | | MHz |
| Slew Rate | $T_A = 25°C$, Unity Gain | 0.3 | 0.7 | | | 0.5 | | | 0.5 | | V/µs |
| Supply Current | $T_A = 25°C$ | | | | | 1.7 | 2.8 | | 1.7 | 2.8 | mA |
| Power Consumption | $T_A = 25°C$ | | | | | | | | | | |
| | $V_S = \pm20V$ | | 80 | 150 | | | | | | | mW |
| | $V_S = \pm15V$ | | | | | 50 | 85 | | 50 | 85 | mW |
| LM741A | $V_S = \pm20V$ | | | | | | | | | | |
| | $T_A = T_{AMIN}$ | | | 165 | | | | | | | mW |
| | $T_A = T_{AMAX}$ | | | 135 | | | | | | | mW |
| LM741 | $V_S = \pm15V$ | | | | | | | | | | |
| | $T_A = T_{AMIN}$ | | | | | 60 | 100 | | | | mW |
| | $T_A = T_{AMAX}$ | | | | | 45 | 75 | | | | mW |

**Note 2:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

**Table 5.7** (*Continued*)

## Electrical Characteristics (Note 5) (Continued)

**Note 3:** For operation at elevated temperatures, these devices must be derated based on thermal resistance, and $T_j$ max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

| Thermal Resistance | Cerdip (J) | DIP (N) | HO8 (H) | SO-8 (M) |
|---|---|---|---|---|
| $\theta_{jA}$ (Junction to Ambient) | 100˚C/W | 100˚C/W | 170˚C/W | 195˚C/W |
| $\theta_{jC}$ (Junction to Case) | N/A | N/A | 25˚C/W | N/A |

**Note 4:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 5:** Unless otherwise specified, these specifications apply for $V_S$ = ±15V, −55˚C ≤ $T_A$ ≤ +125˚C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0˚C ≤ $T_A$ ≤ +70˚C.

**Note 6:** Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

**Note 7:** For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

**Note 8:** Human body model, 1.5 kΩ in series with 100 pF.

## Schematic Diagram
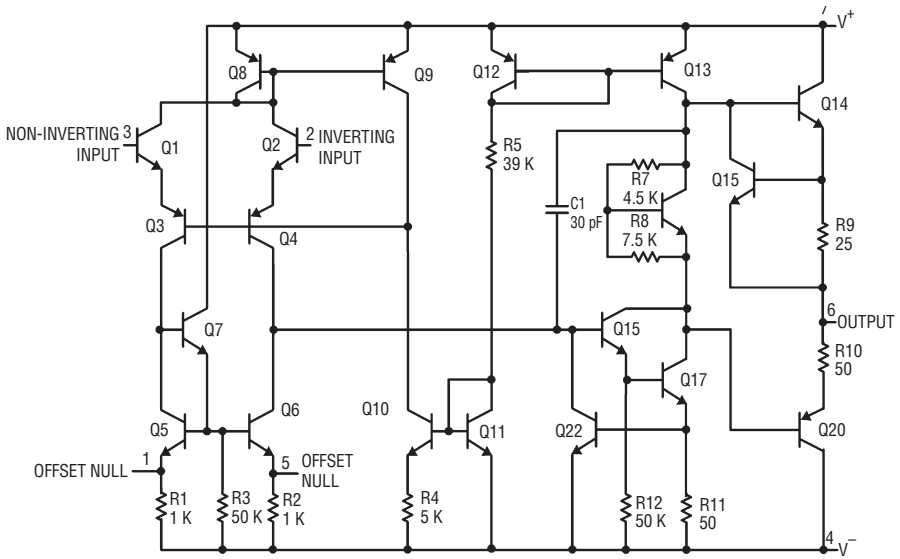


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technological trade-offs. For example, if we want a high-precision op amp with excellent DC parameters and low drift, it will usually not be as fast as an op amp optimized for speed. Unfortunately, it is beyond the scope of this book to get into the op amp integrated circuit design techniques that address such issues in detail.

It is important for the reader to be aware that not all manufacturers publish the exact same list of parameters. There are various reasons for that; one of them is the cost of testing the op amps to guarantee every parameter published. Also not all manufacturers abbreviate or use the same nomenclature for the op amp parameters. It is the job of the op amp user to read very carefully how each manufacturer defines their parameters. For example, for some op amps, you may have a list of the most important parameter like input offset voltage, bias current, offset current, open-loop-gain, and so on, defined with typical, minimum, and maximum values at room temperature, most commonly 25°C/77°F and for +/–15 V power supplies. Then they publish the exact same list of parameters previously mentioned which are valid for their entire operating temperature range, for example, from –40°C to +85°C for +/–15-V power supplies. The important message here is that when one compares op amp or comparator parameters from different manufacturers, it is imperative to read each manufacturer's data sheet very carefully, and become aware of the conditions under which such parameters are being specified. Table 5.7 reproduces an LM741 op amp real data-sheet.

## 5.8  SUMMARY

This chapter is an overview of some of the most commonly used op amp-based circuits. Generally speaking, circuit designers use the op amp transfer functions derived, assuming the op amp is an ideal element. Most times that is correct for most routine applications. A routine application is one that is not high-precision demanding, or very high speed, or extremely low noise for example. However, when one designs highly sophisticated op amp applications, more care has to be paid and use the op amp model with the parameters that are most important for such application. One should model op amps introducing most important electrical parameters for the application. As an example, if one is interested in a high DC precision application, offset voltage, current, and bias currents should be introduced into the model; however, parameters like the gain-bandwidth product is certainly not important because the signals we are dealing with are DC signals. Conversely, if we have a very high speed, AC-coupled op amp application, certainly gain-bandwidth product is of utmost importance, while DC parameters are not important. Why are DC parameters not important? Because if an op amp is AC-coupled, that means that the input signals into the op amp as well as the output signal are

capacitively coupled to their respective front-end and back-end stages, thus blocking the DC and AC errors due to offsets.

## FURTHER READING

1. Sergio Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, McGraw-Hill, New York, 1988.

2. Walter G. Jung, ed., *Op Amp Applications*, Analog Devices, Norwood, MA, 2004.

3. Robert F. Coughlin and Frederick F. Driscoll, *Operational Amplifiers and Linear Integrated Circuits*, Prentice Hall, Englewood Cliffs, NJ, 1991.

4. Hank Zumbahlen, ed., *Basic Linear Design*, Analog Devices, Norwood, MA, 2007.

## PROBLEMS

**5.1**  Mention five ideal operational amplifier parameters.

**5.2**  Using linear-dependent current or voltage-controlled sources, establish models for the following linear amplifiers:

    **(a)**  Voltage amplifier

    **(b)**  Current amplifier

    **(c)**  Trans-conductance amplifier

    **(d)**  Trans-resistance amplifier

**5.3**  Explain in your own words why a voltage amplifier features $R_i \to \infty$, $R_o = 0$, and $A_v = v_o / v_i$.

**5.4**  Explain in your own words why a current amplifier features $R_i = 0$, $R_o \to \infty$, and $A_I = i_o / i_i$.

**5.5**  Explain in your own words why a trans-conductance amplifier features $R_i \to \infty, R_o \to \infty$, and $A_G = i_o / V_i$.

**5.6**  Explain in your own words why a trans-resistance amplifier features $R_i = 0$, $R_o = 0$, and $A_R = v_o / i_i$.

**5.7**  Design an ideal op amp-based amplifier that has a gain of −2; draw the circuit.

**5.8**  Implement an ideal op amp-based circuit that produces the following arithmetic operation:

$$V_{out} = -V_1 + 3\,V_2. \qquad\qquad (5.103)$$

In Equation (5.103) $V_1$ or $-V_1$ can be used as an input voltage, so is $V_2$, but not $(3\,V_2)$. Implement the circuit with the smallest number of op

**Table 5.8   Table for Problem 5.9: inverting amplifier with finite $A_{OL}$**

| Open-Loop Gain ($A_{OL}$) | Ideal Closed-Loop Gain ($A_{OL} \to \infty$) (dB) | Closed-Loop Gain (CLG) Accounting for Finite $A_{OL}$ | Absolute Error = CLG − ICLG | Relative Error = (CLG − ICLG) × 100/CLG (%) |
|---|---|---|---|---|
| 1000 | −2 | | | |
| 10,000 | −2 | | | |
| 100,000 | −2 | | | |
| 1,000,000 | −2 | | | |
| 1,000 | −20 | | | |
| 10,000 | −20 | | | |
| 100,000 | −20 | | | |
| 1,000,000 | −20 | | | |

amps and explain why you can, or cannot implement it differently (i.e., with more or less op amps).

**5.9**  Assume that you have an op amp-based inverting amplifier; assume that the op amp used is ideal except for its gain. Complete Table 5.8 knowing the op amp open-loop gain and the ideal op amp-based inverting amplifier CLG. Refer to Table 5.8's first and second columns from the left.

**5.10**  For the circuit given in Figure 5.31, calculate the value of the output voltage $V_{OUT}$. Assume an ideal op amp.

**5.11**  For the circuit given in Figure 5.32, calculate the value of the output voltage $V_{OUT}$. Assume an ideal op amp.

**5.12**  Assume that you have an op amp in buffer amplifier configuration. The buffer CLG is 1 assuming an ideal op amp. Now assume the open-loop gain of the op amp ($A_{OL}$) is finite. For finite open-loop gains of $10^3$, $10^4$, $10^5$, and $10^6$ determine the CLG of the buffer amplifier and the relative error in ppm (parts per million).

**5.13**  Implement with the smallest possible number of ideal op amps the following analog expression:

$$V_{out} = K_1 V_1 + K_2 \int V_2 dt + K_3 \frac{dV_3}{dt}, \qquad (5.104)$$

where $K_1$, $K_2$, and $K_3$ in Equation (5.103) are arbitrary constants. $V_1$, $V_2$, and $V_3$ are input voltages that vary with respect to time, and $V_{out}$ is the total output voltage as shown by Equation (5.104). Hint: It is fine to use resistors and capacitors in addition to the op amps.
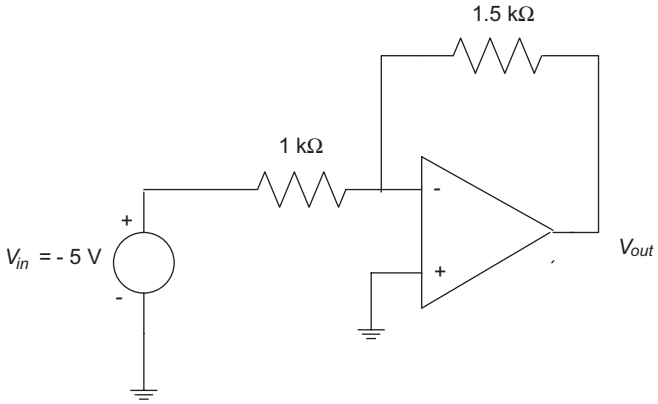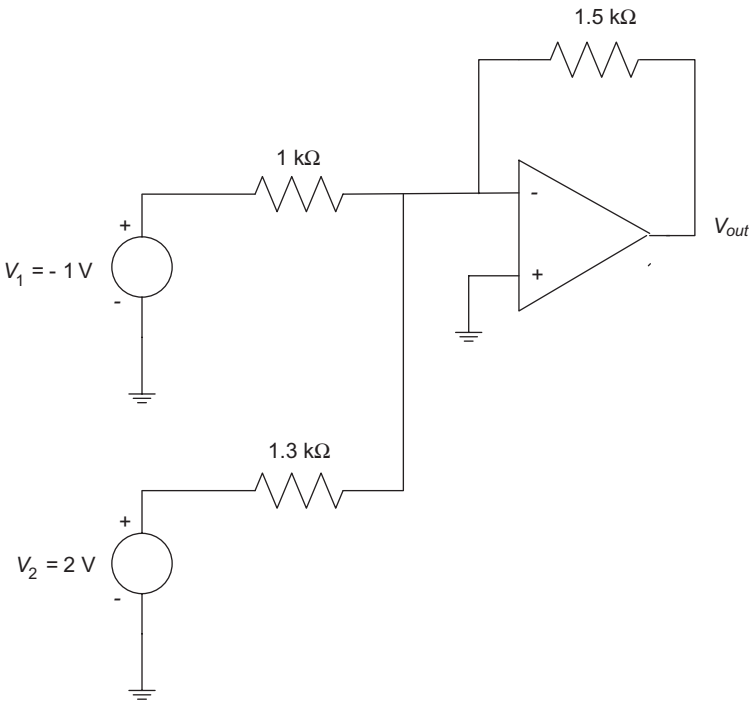
**Figure 5.31** For Problem 5.10.
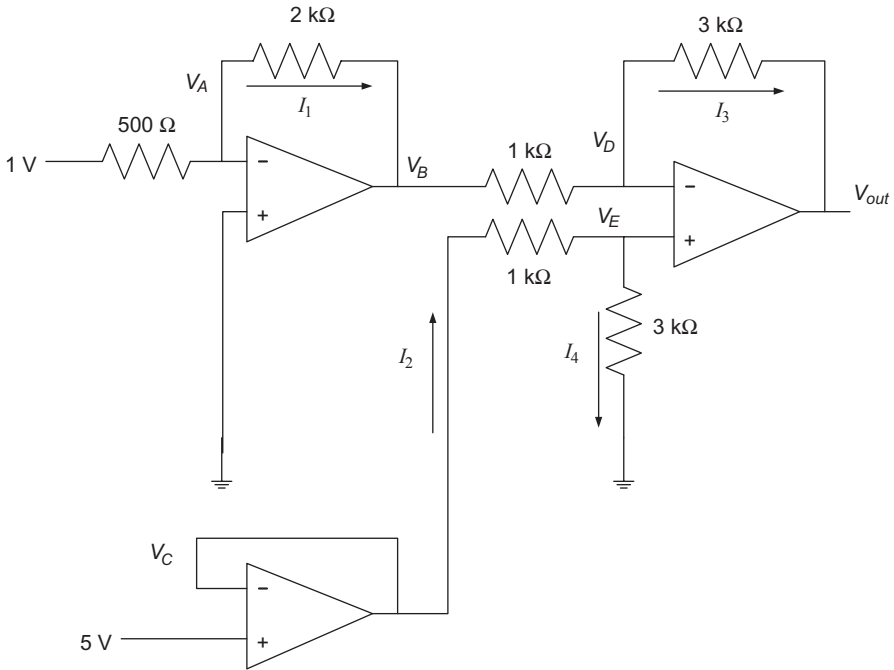


**Figure 5.32** For Problem 5.11.

**Figure 5.33**  For Problem 5.15.

**5.14**  Find an alternate manner, also using ideal op amps, of implementing Equation (5.104). Hint: It is fine to use resistors and capacitors in addition to the op amps.

**5.15**  Given the circuit of Figure 5.33 calculate (a) $V_{out}$, (b) $V_A$, (c) $V_B$, (d) $V_C$, (e) $V_D$, (f) $V_E$, (g) $I_1$, (h) $I_2$, (i) $I_3$, and (j) $I_4$. Assume ideal op amps. Do not change the assumed directions for the currents.

**5.16**  Given the circuit of Figure 5.34 determine the circuit transfer function: $V_{out} (j\omega)/V_{in} (j\omega)$. Note: Express the final transfer function as a ratio of binomials with zeros and poles. Zeros are referred to as the numerator roots or zeros. Poles are referred to as the denominator roots or zeros.

**5.17**  For the circuit of Figure 5.34 assume the following component values: $R_1 = 1\ k\Omega$, $C_1 = 1\ \mu F$, $R_2 = 10\ k\Omega$, and $C_2 = 100\ pF$. Draw the asymptotic magnitude and phase Bode plots from 1 Hz to 1 MHz.

**5.18**  For the circuit of Figure 5.34 assume the following component values: $R_1 = 1\ k\Omega$, $C_1 = 1\ \mu F$, $R_2 = 10\ k\Omega$, and $C_2 = 100\ pF$. Draw the exact magnitude and phase Bode plots from 1 Hz to 1 MHz. Only calculate magnitude and phase values for 1 Hz, 10 Hz, . . . , 1 MHz.
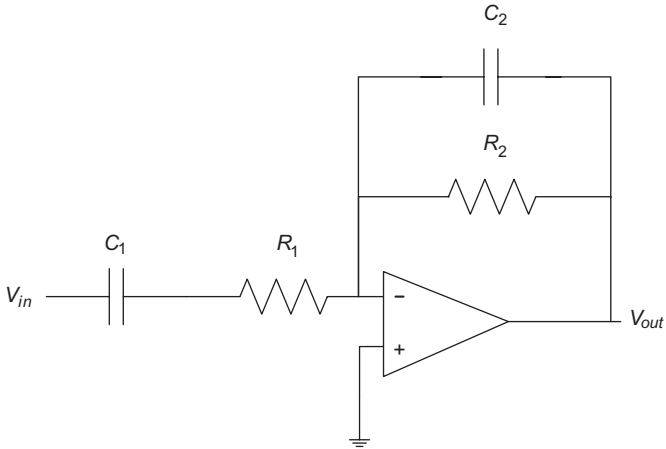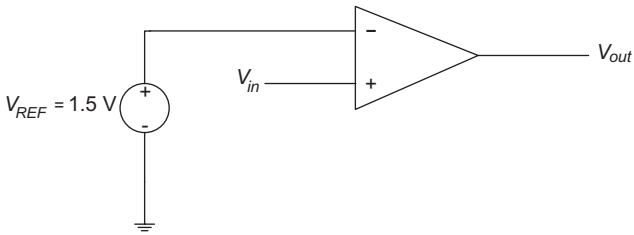
**Figure 5.34** For Problems 5.16, 5.17, and 5.18.



**Figure 5.35** For Problem 5.19.

**5.19** For the circuit of Figure 5.35 determine (a) $V_{out}$ for $V_{in} = -1$ V, (b) $V_{out}$ for $V_{in} = 0$ V, (c) $V_{out}$ for $V_{in} = 1$ V, (d) $V_{out}$ for $V_{in} = 2$ V, (e) $V_{out}$ for $V_{in} = 3$ V. (f) Also for all five cases (a) through (e), calculate the voltage difference: $V_{in} - V_{REF}$

**5.20** Research problem: Using Web sites of some op amps and comparator manufacturers, determine the fundamental differences between real-life operational amplifiers and comparators. Examples of some manufacturers are: http://www.linear.com, www.intersil.com, http://www.ti.com, and http://www.analog.com
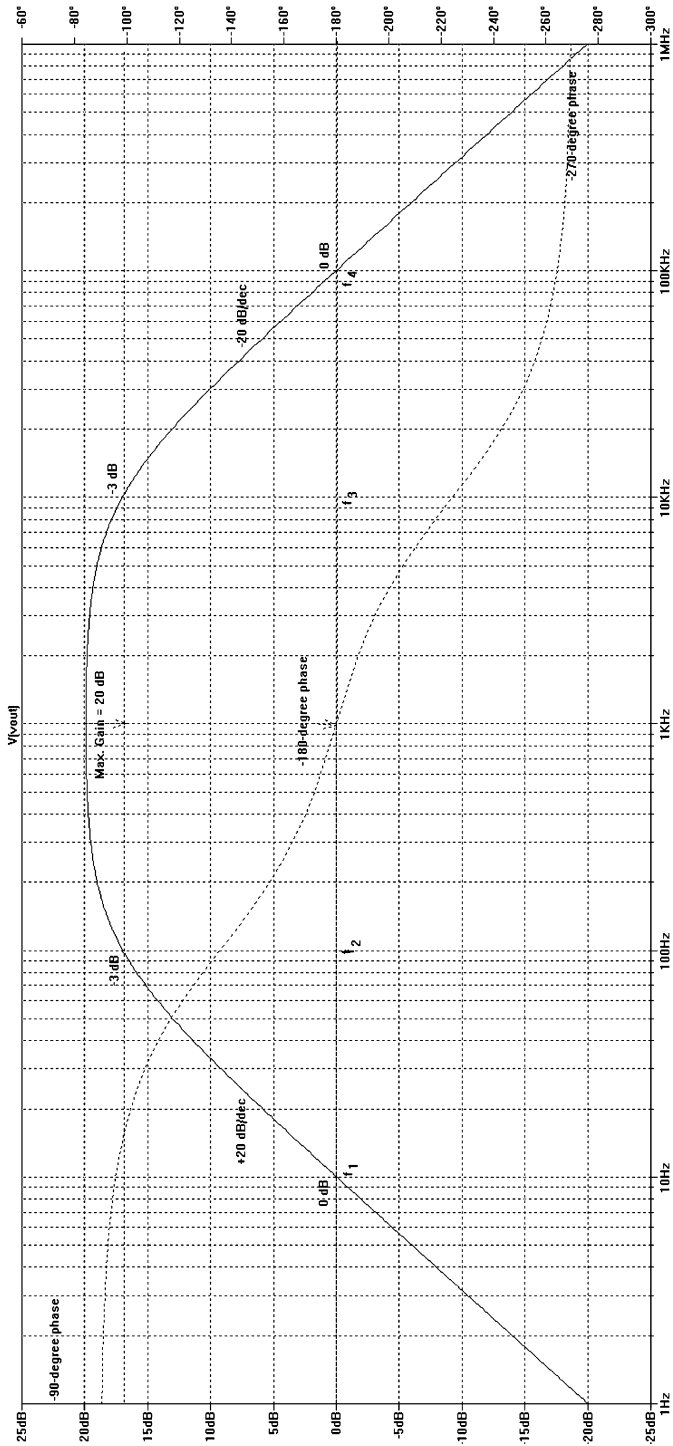
**Figure 5.22** Exact Bode plots of a practical differentiator, integrator, and band-pass filter.