Power Electronics Semiconductor Devices
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Chapter 2

Insulated Gate Bipolar Transistors

2.1. Introduction

MOSFETs and bipolar power transistors show complementary characteristics. On the one hand, bipolar junction transistors (BJT) show a low voltage drop, mainly for high voltage devices; however, the base drive needs a drive current, and they are weak close to their limits. On the other hand, power MOSFETs are very fast for switching operations, strong in overload operations, and the gate drive only requires very low energy (a voltage drive). However, for high voltage devices, MOSFET internal resistance is high, leading to a large voltage drop. As the useful characteristics of both BJTs and MOSFETs were required, manufacturers conjugated the two to create a new device, the insulated gate bipolar transistor (IGBT). After 20 years of consistently good performance IGBT was close to having a monopoly on the market of high voltage applications, from 1 kV to 8 kV, also replacing GTO for some applications.

Devices from a few amps to kilo-amps are today allowable on the market, in several packages. Good adaptation between IGBTs and applications is also allowable: some IGBTs have a low voltage drop but quite slow commutations, while other devices are very fast, with a higher voltage drop.

Chapter written by Pierre ALOÏSI.

2.2. IGBT technology

2.2.1. *IGBT structure*

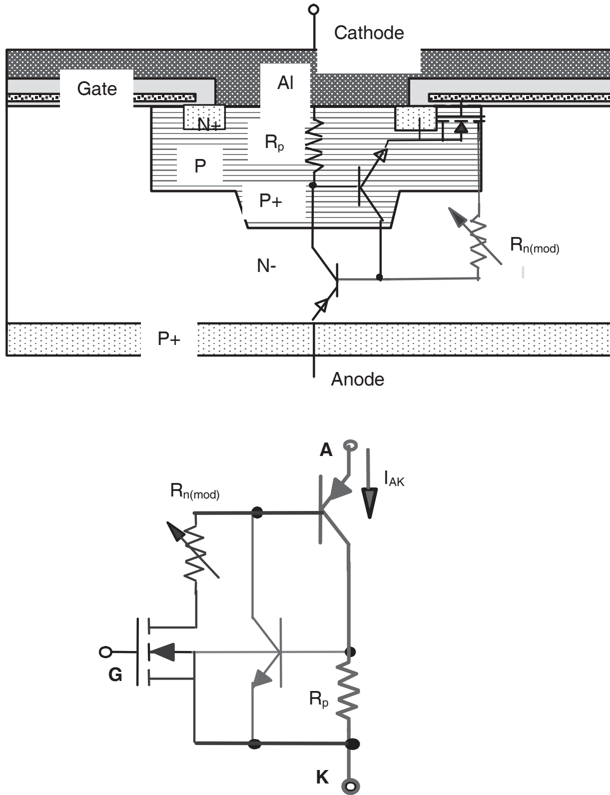


Figure 2.1. *IGBT structure*

Figure 2.1 shows the vertical section of an IGBT: it is like a power MOSFET construction, but N+ MOS substrate is replaced by a highly doped P+ substrate. The new P+ N- junction injects some holes into the N- drift zone, which is modulated by electrons coming from the channel. The equivalent circuit is also shown in Figure 2.1, where the parasitic JFET and the internal capacitances are not revealed. The main elements of the structure are:

– the bipolar PNP where the emitter is the P+ layer (IGBT anode or collector), the base is the drift zone N- layer, and the P+ well is the collector;

– the NPN parasitic transistor where the emitter is the N+ source (IGBT cathode or emitter), the base is the P+ well, and the collector is the N- zone;

– two resistances, R_p and R_{mod}, which are the resistance of the Pwell under the source, and modulated resistance of the N- drift zone;

– the channel.

The two NPN and PNP transistors are connected in such way that they represent a four layer structure, called a thyristor. This is a positive feedback device, which means that once started, it cannot be switched off. As this is the case, the thyristor should not be switched on, in order to avoid any IGBT failure. There are two possible options for avoiding IGBT failure.

The first option is to set the gain of the PNP transistor at only the value requested for the IGBT main characteristics, and dramatically reduce the sheet resistance R_p, in order to maintain the veracity of the following inequality:

$$R_P \cdot I_{C(PNP)} = R_P \cdot \frac{\beta_{PNP}}{1+\beta_{PNP}} \cdot I_{C\max} < 0.6\ V$$

which gives $$R_P < \frac{1+\beta_{PNP}}{\beta_{PNP}} \cdot \frac{0.6}{I_{C\max}}$$

I_{Cmax} is the thyristor latching current. Beyond it, IGBT switch-off is impossible, and the device is destroyed.

R_p reduction requires a shorter source length, with a higher Pwell doping level. P/P+ diffusion technique allows increased doping levels between and under sources, keeping the adequate channel doping level in line with the threshold voltage, Vth.

A second way is to reduce the I_C(PNP) current through R_p by decreasing the gain of the PNP transistor, β_{PNP}. But this gain sets the injection levelof the holes, and consequently the resistivity modulation in the N- drift zone. So, the device designer has to make a compromise: a low gain to cancel the thyristor operation or a high gain for low V_{CEsat}.

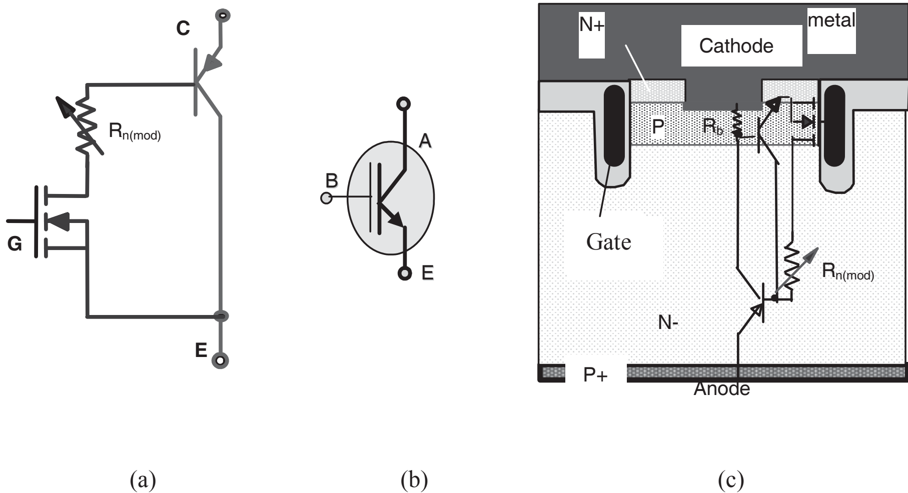


Figure 2.2. *IGBT equivalent circuit, symbol and trench gate IGBT*

Figure 2.2 shows the IGBT equivalent circuit, when the NPN transistor is technologically cancelled, and the series resistance R_p is very low. A bipolar PNP transistor remains, driven by a MOSFET with an internal resistance, R_{MOD}. The common IGBT symbol is also shown.

This equivalent circuit shows that the MOSFET is always a low voltage MOSFET, connected between the PNP transistor base and the collector. Load current is divided between MOS and the bipolar transistor: meaning a very low MOSFET R_{dson} is welcomed to obtain a low IGBT V_{sat}. Today, most IGBTs are built with a trench gate MOSFET (see Figure 2.2c). The Pwell is a very thin layer, short-circuited by the source (emitter) metallization. Thus, on modern IGBTs, R_p is close to zero.

2.2.2. *Voltage and current characteristics*

It is mainly the PNP bipolar transistor, with an opened base, that gives the IGBT maximum voltage. When a supply voltage is applied on the IGBT, the drift zone is divided into two regions. The first region, W_m, is close to the IGBT collector, and has a weak injection level, due to the PNP emitter-base junction forward polarization. A second region, W_{ZD}, is a space charge region, close to the MOSFET (PNP collector), and is a product of the junction P+N- reverse polarization, (see Figure 2.3). Total current I_A, at the space charge output, is the sum of two currents: a

generation current I_{gen} in the space charge region, and an injected current from the weak injection region in the space charge. This is then multiplied by M in the space charge region, as seen in the following equation:

$I_A = \gamma_{PE}.\alpha_{Tm}.I_A.M + I_{gen}.M$ which gives: $I_A = I_{gen}.M.(1-\gamma_{PE}.\alpha_{Tm}.M)^{-1}$

where γ_{PE} is the P+N-P transistor emitter injection coefficient, and α_{Tm} is the effective base W_m transport coefficient, with a low injection level, less than one. Actually, it represents the ratio between the hole current at the output and at the input region W_m:

$$a_{Tm} = \frac{1}{\cos\frac{W_m}{L_p}}$$

where L_p is the hole diffusion constant in the $W_{m.}$ region.

When $\gamma_{PE}.\alpha_{Tm}.M > 1$, avalanche occurs giving

$$M = (\gamma_{PE}.\alpha_{Tm})^{-1}.$$

If the well known expression:

$$M = \left[1 - \left(\frac{V_{app}}{V_{DSS}}\right)^n\right]^{-1}$$

is used, the ratio between the two structures sustaining voltages, V_{CES} for PNP transistor and V_{DSS} for MOSFET is:

$$V_{CES} = (1 - \gamma_{P_E}.\alpha_{Tm})^{\frac{1}{n}} \cdot V_{DSS}$$

where n is between 4 and 6 for a P+N junction, and between 2 and 4 for the N+P junction.

Thus, the IGBT sustaining voltage is slightly less than that of a MOSFET with the same N- thickness.

For example: if $\gamma_{PE} = 0.8$ and $\alpha_{Tm} = 0.5$, $V_{CES} = 0.8V_{DSS}$ with $n = 5$

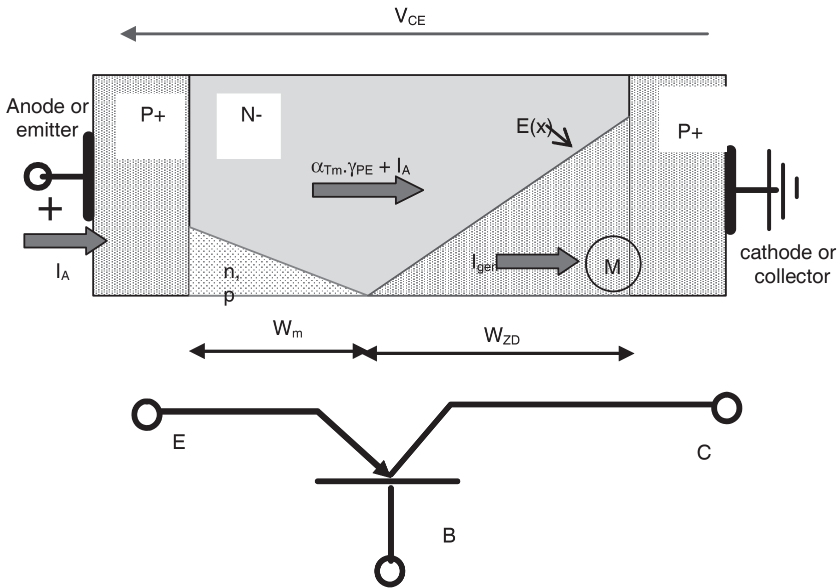


Figure 2.3. *IGBT static sustaining voltage*

The thermal aspects of the system mainly define the maximum current limitation for both IGBT and power MOSFET. Current density in the IGBT is larger when the voltage drop and thermal resistance are lower. If the following equation is true:

$$J_{AK} = \frac{T_j - T_{env}}{R_{th(j-c)} V_{AK}}$$

the theoretical current density is around 330 A.cm^{-2}, for:

– a silicon maximum temperature of T_j = 150°C,

– an ambient temperature T_{amb} = 50°C,

– a thermal resistance per square centimeter of silicon of 0.1°C/W (quite impossible to obtain),

– and a voltage drop of 3 V.

Normally, in a 1,000 V IGBT, the maximum current density is around 50 to 150 A.cm^{-2}, and 100 to 200 A.cm^{-2} in a 600 V IGBT. Recall that the current density in a 1,000 V power MOSFET is only a few A.cm^{-2}.

2.3. Operation technique

2.3.1. *Basic principle*

IGBTs are used in bipolar power devices. Two types of carriers, holes and electrons, transport the current through the drift zone of the device. The channel drives electrons when a gate voltage over the threshold voltage is applied. The anode P+N- junction injects holes when a positive voltage is applied between the anode and cathode of IGBT. Electrons and holes move in opposite directions inside the drift zone, electrons to the anode and holes to the cathode. At the end of N- drift zone, some of the electrons enter the P+ anode. Simultaneously, some of the holes come into the Pwell. The difference between incoming and outgoing electrons, discounting recombination, is the Q stored charge in the drift zone. Because of electrical neutrality, the difference between holes is the same as the difference between electrons; these stored charges modulate the drift zone in the on-state. Figure 2.4 shows this exchange of charges in the on-state IGBT.

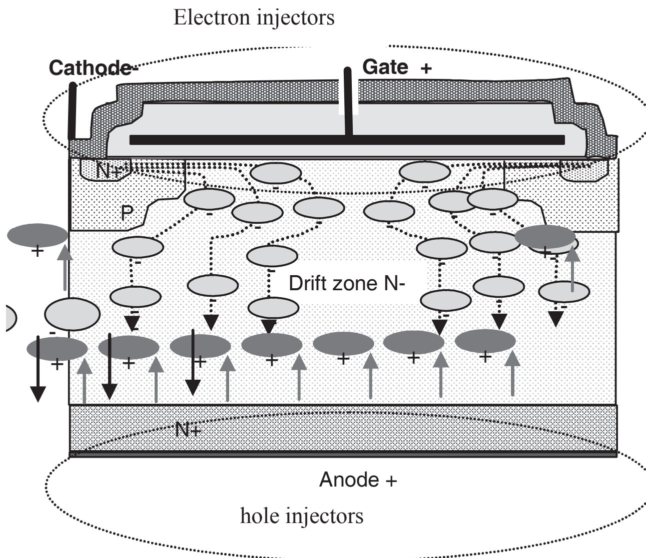


Figure 2.4. *Charge injection during on-state*

At switch-off, gate voltage decreases, and the electron injection stops when the gate voltage becomes lower than the threshold voltage V_{th}. In order to really switch-off the IGBT, stopping the electron injection is not enough, the stored charge Q (electrons and holes in equal quantity) must also be cleared out. Removal of these

charges (sometimes called "trapped charges") at the PNP base is impossible, because it opens when MOS is switched off. Thus, they should recombine on site (see Figure 2.5).

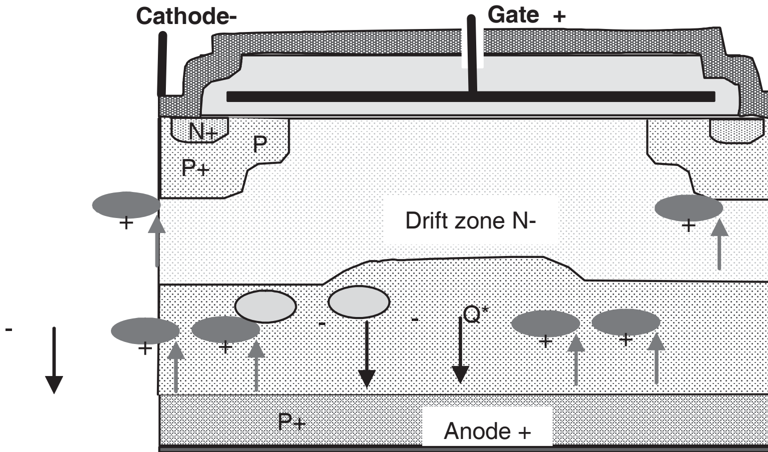


Figure 2.5. *Recombination of charges during switch-off*

2.3.2. *Continuous operation*

During "on" time, the load imposes an anode current I_A equal to the cathode current. Inside the device, this cathode current is driven by the electron current coming from the channel, and the hole current coming from the drift zone and P+ well. The anode current is comprised of the electron current coming from the drift zone, and the hole current coming from the PNP emitter. Stored charge Q is created by the difference between electrons coming from the channel and those entering in the P+ injector (or by the difference between the holes coming from the PNP emitter and those entering the Pwell), minus the electrons (or holes) recombined on site. If $J_{n(K)}$ and $J_{P(K)}$ are the current densities at the cathode end and $J_{n(A)}$ and $J_{P(A)}$ are the current densities at the anode end, the stored charge per square centimeter is:

$$Q^* = \tau.(J_{n(K)} - J_{n(A)}) = \tau.(J_{p(A)} - J_{p(K)})$$

where τ is the unique recombination rate for electrons and holes, blended by the carrier lifetime.

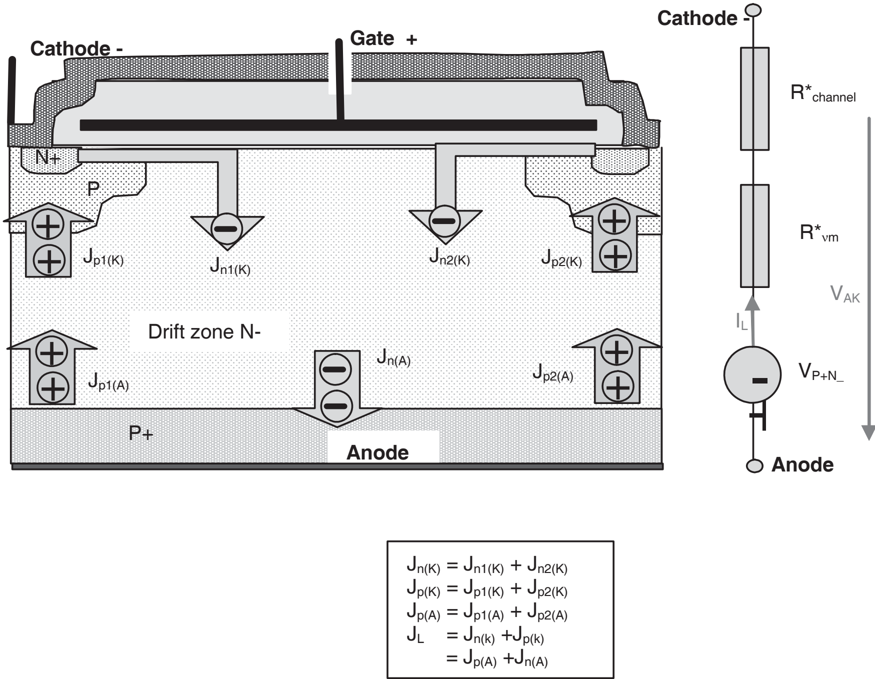


Figure 2.6. *Charges moving in the on-state IGBT and the equivalent circuit*

The IGBT voltage drop, V_{AK}, is composed of the channel voltage, $V_{channel}$ (close to the $R_{channel}.I_L$), and the modulated drift zone voltage, $V_m \approx R_{vm}.I_L$, by the hole injector voltage V_{P+N-} (see Figure 2.6). Channel voltage is the same as for a MOS:

$$R_{channel} \approx \left[\frac{Z}{L} \mu_{ns} \frac{\varepsilon_{ox}}{d_{ox}} (V_{GS} - V_{th}) \right]^{-1}$$

Calculation of V_m and V_{P+N-} is more difficult and requires not only the stored charge quantity, but also the charge profile in the drift zone. Numerical expressions are requested. Figure 2.7 shows two possible profiles versus gain, $\beta_{PNP} = J_P(W_\nu)/J_n(W_\nu)$. For $\beta_{PNP} > 1/b$ (where b is the ratio between electron mobility and hole mobility; $b \approx 3$), we can admit, neglecting the carrier concentration, $p(W_\nu)$, that the carrier distribution is triangular, according to Figure 2.7c. In this case, the stored charge density and the drift zone resistance per square centimeter of silicon may be estimated by the equation:

$$R^*_{vm} = \frac{1}{q(1+b)\mu_n} \int_0^{W_v} \frac{1}{N_D + p(x)} dx = \frac{W_v{}^2}{2(1+b)\mu_n Q^*} \cdot \ln(1 + \frac{2Q^*}{qN_D W_v})$$

where γ_p and γ_n are the injection coefficients for holes and electrons, defined by the two following expressions:

$$\gamma_p = \frac{J_p(0)}{J_A} \qquad \text{and} \qquad \gamma_n = \frac{J_n(W_v)}{J_A} = \frac{J_{Channel}}{J_A}$$

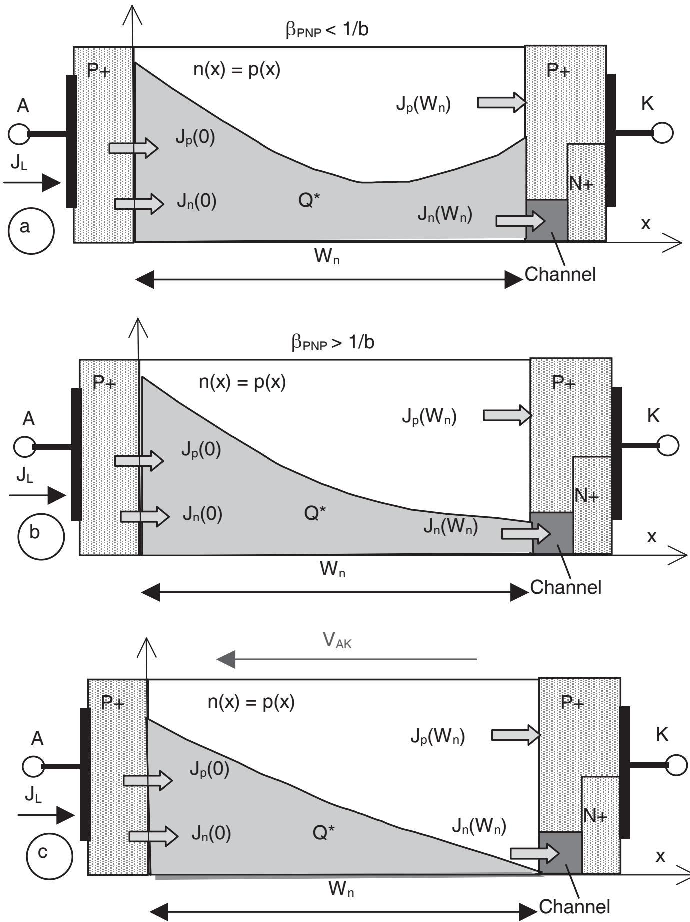


Figure 2.7. *Charge distribution in the drift zone*

Figure 2.8 shows an example of drift zone resistance modulation, R^*_{vm}, by the stored charges Q*. The following numerical values were used: $N_D = 10^{14}$ cm^{-3}, μ_n = 1,000 cm^2 V^{-1}s^{-1}, W_v = 100 µm. We can clearly see that the resistivity is divided by a factor greater than 100, for a stored charge density of 1 µC.cm^{-2}. Now, we can also see that the stored charge must be controlled, because, over a defined level of charge the modulation effect is reduced even with a large quantity of charges. The internal hole injector voltage V_{P+N-} may be estimated using the following equation:

$$V_{P^+N^-} = U_T \ln(1 + \frac{p(0)N_D}{n_i^2}) = U_T \ln(1 + \frac{2Q^* N_D}{qW_v n_i^2})$$

This value is set from 0.5 V to around 1 V.

Three methods exist for the control of stored charges: by recombination rate τ, by holes injection coefficient γ_P, and by electron injection coefficient γ_n. The recombination rate control is achieved by injecting a heavy metal (gold or platinum) into the N- drift zone, or by electron irradiation. The goal of these techniques is to provide some recombination centers for trapped charges.

The electron injection coefficient of electron injector, γ_n, set at a high level in order to avoid any parasitic thyristor switch-on, and in order to control the channel voltage drop. Recombination is improved by controlling the hole injector γ_P on the anode. Two methods are in competition: “punch through” and “non-punch through” technologies (see Figure 2.9).

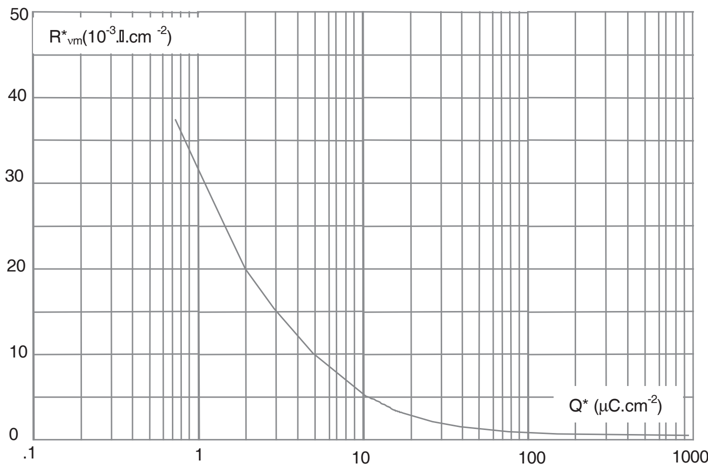


Figure 2.8. *R_{vm} modulation resistance by charge injection: example*

Punch through (PT) technology is directly designed from the power MOSFET technology, where the N+ substrate is replaced by a P+ substrate, with a thickness of approximately 300 µm. The N- drift zone is created by an epitaxy technology. A N+ buried layer, W_N, with a thickness of a few microns, is grown by epitaxy between the P+N- junctions, to insure the control of the injection coefficient, γ_P.

Without a buried layer, the N- drift zone must be thick enough in order to prevent the electric field from rising to the P+ anode layer, under maximum voltage. This buried layer allows the electric field to be inside a thinner N- drift zone, W_ν. This buried layer gives the PT-IGBT an asymmetric voltage.

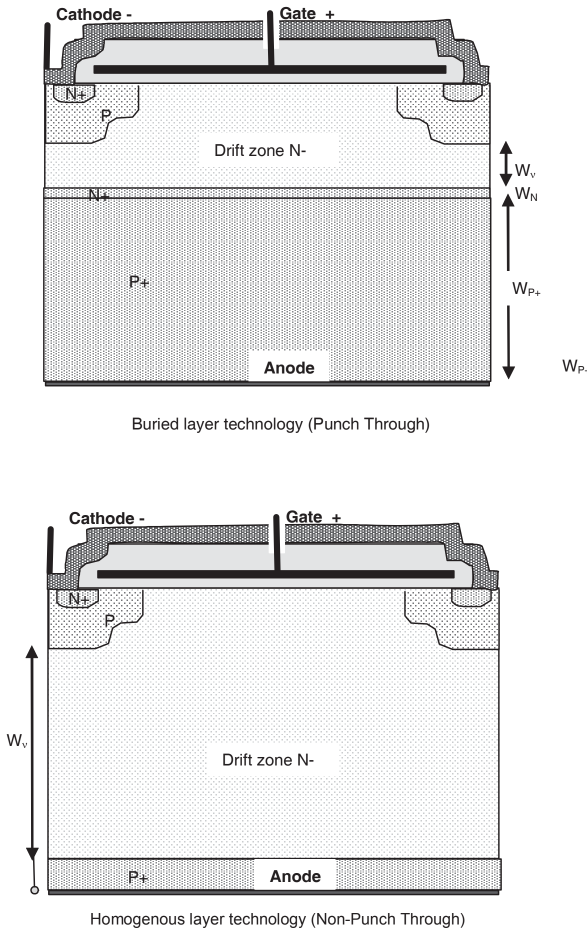


Figure 2.9. *Two IGBT technologies*

Figure 2.10 shows the electric field inside the drift zone under the maximum voltage of the device, both with and without the buried layer.

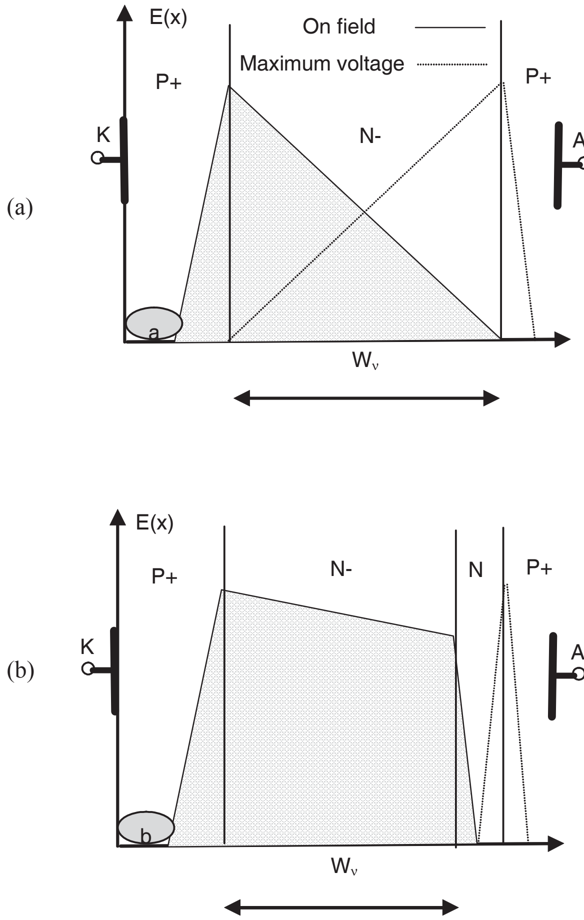


Figure 2.10. *Electric field in the drift zone*
a) without buried layer; b) with buried layer

The W_N thickness and the doping level N of the buried layer are the two parameters for the control of the injection coefficient, γ_P. This is lower when the layer is thicker, and its doping level higher.

Its value is given by the following approximate equation:

$$\gamma_p = \frac{qD_{pN}}{J_A L_{pN} \sinh \frac{W_N}{L_{pN}}} \cdot \left(\frac{{p_{N^-}}^2}{N} \cdot \cosh \frac{W_N}{L_{pN}} - p_N\right)$$

where L_{PN} and D_{PN} represent respectively the length and the hole diffusion constant in the buried layer, P_N represents the hole concentration in the buried layer (assuming the design has a weak doping level) to the P+ anode contact, and P_{N-} represents the hole (or electron) concentration in the drift zone (assuming the design has a high doping level) to the buried layer contact (see Figure 2.11a).

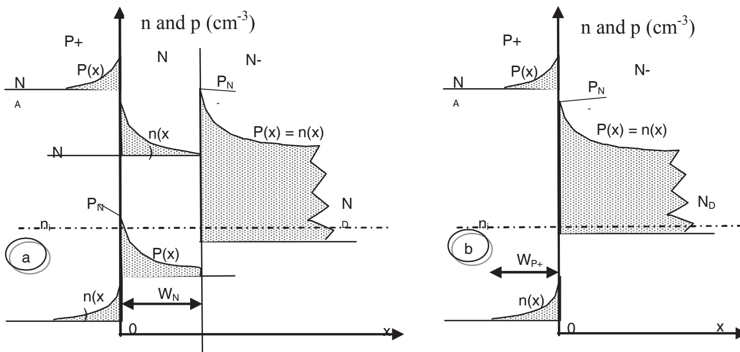


Figure 2.11. *Hole injection control:*
a) by buried layer W_N; b) by W_{p+} thickness

In the NPT-IGBT, the N- drift zone is installed in the overall wafer width, in order to keep a sufficient stiffness: this is at least around 200 µm. This thickness can sustain around 2,000 V. So, a medium voltage IGBT, approximately 1,200 V, is penalized for its forward voltage drop. “Thin wafer” manufacture will be a solution. The P+ anode is made with a boron diffusion or an implantation with small thickness (less than 1 µm). Stored charge is controled by the injection coefficient γ_p, set by the P+ anode thickness. The recombination coefficient is kept high in order to have a modulation in the whole part of the N- zone. γ_p is given by the following equation:

$$\gamma_p = 1 - \frac{qD_{nP^+}}{W_{P^+}} \cdot \frac{{p_{N^-}}^2}{N_A} \cdot \frac{1}{J_A}$$

where D_{nP+}, N_A, P_{N-} represent respectively, the electron diffusion constant in the P+ anode, the doping level of the anode and the charge concentration in the drift zone to anode contact (see Figure 2.11b).

2.3.3. *Dynamic operation*

The dynamic operation of IGBT is much more complex than in MOSFET operation, because the IGBT mechanism is a mix of capacitive operation, like MOSFET and bipolar operation. Also, the N- drift zone cannot be split into several regions of different natures. For example, a highly modulated region and space charge, a lowly modulated region and a space charge region, a highly modulated region and a space charge, with a neutral region between. All these combinations depend on the switching conditions even during the same switching evolution.

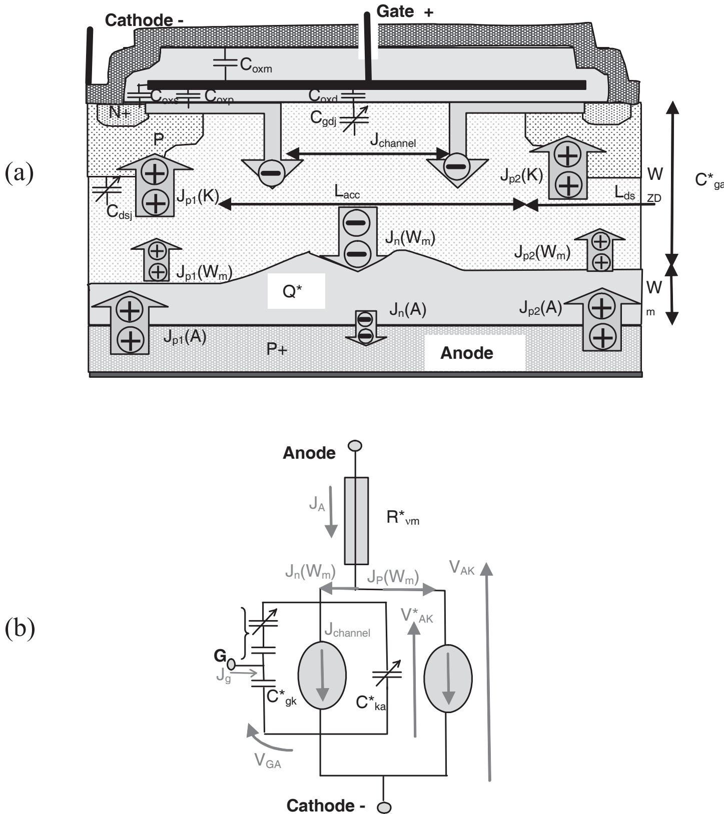


Figure 2.12. *IGBT dynamic operation:*
a) internal elements; b) equivalent circuit

Figure 2.12a shows, for example, the IGBT internal state with a high level modulated region, W_m, and a space charge, W_{ZD}. It represents the IGBT internal state during hard switching, with an inductive load. Figure 2.12b shows the equivalent circuit for the same state, with similar elements as in a power MOSFET. Under switching conditions, the voltage drop inside the modulated region is low, so the IGBT voltage drop is equal to this space charge voltage:

$$V_{AK}(t) = V^*_{AK}(t).$$

In this case, with the equivalent circuit, the following equations may be written as an IGBT model for a hard switching operation:

$$(C^*_{AK} + C^*_{GA})\frac{dV_{AK}}{dt} - C^*_{GA}\frac{dV_{GK}}{dt} = \frac{1}{1+\beta_{PNPm}}J_A - J_{Channel}$$

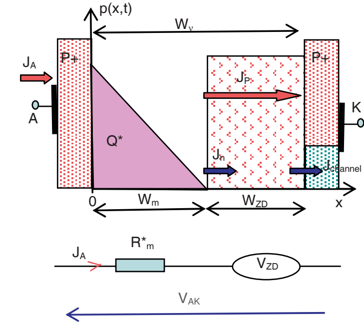
$$(C^*_{GK} + C^*_{GA})\frac{dV_{GK}}{dt} = C^*_{GA}\frac{dV_{AK}}{dt} + J_g$$

$$\frac{dQ(t)^*}{dt} = -\frac{Q(t)^*}{\tau} + J_{p(A)} - J_{p(W_m)} = -\frac{Q(t)^*}{\tau} + (\gamma_p - \frac{\beta_{PNPm}}{1+\beta_{PNPm}}) \cdot J_A$$

$$W_m = W_v - \sqrt{\frac{2\varepsilon_{Si}V_{AK}}{qN_D}}$$

where β_{PNPm} is the PNP dynamic gain, with a real base $W_m(t)$, which changes during switching operation.

Using these equations, we can see that the current or voltage speeds can be driven by the channel current, and thus by the gate drive. With the hypothesis of a linear distribution of charges in the modulated region, Table 2.1 shows a mono-dimensional analytically simplified model of the drift zone for the following three cases: a high modulated region and a space charge region, a high modulated region and a neutral region, a high modulated region and a neutral region and a space charge region. These represent the approximate states of the drift zone in the power electronics applications.



$$V_{drift}(t) = V_{ZD}(t) \text{ and } J_A(t) = J_{channel}(t) + J_P(W_m,t)$$

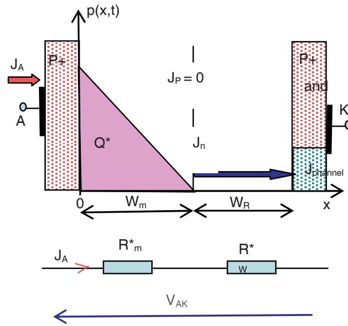
$$J_n(W_m,t) = \frac{b}{1+b} J_A(t) - qD\frac{p(0,t)}{W_m(t)} - J_{dep}(W_m,t)$$

$$J_P(W_m,t) = \frac{b}{1+b} J_A(t) + qD\frac{p(0,t)}{W_m(t)} + J_{dep}(W_m,t)$$

$$J_{dep}(W_m,t) = \frac{Q^*(t)}{3W_m(t)qN_D}.C^*_{ZD}\frac{dV_{ZD}(t)}{dt}$$

$$J_{channel}(t) = J_n(W_m,t).C^*_{ZD}\frac{dV_{ZD}(t)}{dt}$$

$$C^*_{ZD} = \sqrt{\frac{q\varepsilon_{si}N_D}{2V_{ZD}(t)}} \quad \text{and} \quad Q^*(t) = \frac{1}{2}qW_m(t)p(0,t)$$



$$V_{drift}(t) \approx [R^*_m(t) + R^*_W(t)]J_A(t)$$

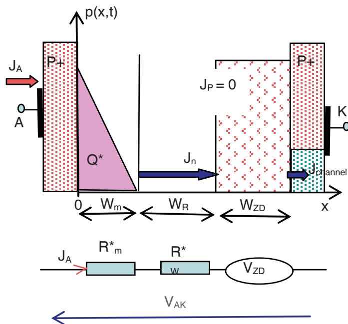
$$J_A(t) = J_{channel}(t)$$

$$R^*_W(t) = \frac{1}{q\mu_n N_D}.W_R$$

$$R^*_m(t) = \frac{1}{q\mu_n(1+b)}.\int_0^{W_m}\frac{1}{N_D + p(x,t)}dx$$

$$p(x,t) = p(0,t)\left[1 - \frac{x}{W_m(t)}\right]$$

$$Q^*(t) = \frac{1}{2}qW_m(t)p(0,t) \text{ and } \frac{dQ^*(t)}{dt} = -\frac{Q^*(t)}{\tau} + J_A(t)$$



$$V_{drift}(t) \approx [R^*_m(t) + R^*_W(t)]J_A(t) + V_{ZD}(t)$$

$$J_A(t) = J_{channel}(t) + C^*_{ZD}\frac{dV_{ZD}(t)}{dt}$$

$$R^*_W(t) = \frac{1}{q\mu_n N_D}.W_R$$

$$R^*_m(t) = \frac{1}{q\mu_n(1+b)}.\int_0^{W_m}\frac{1}{N_D + p(x,t)}dx$$

$$p(x,t) = p(0,t)\left[1 - \frac{x}{W_m(t)}\right]$$

$$Q^*(t) = \frac{1}{2}qW_m(t)p(0,t) \quad \text{and} \quad \frac{dQ^*(t)}{dt} = -\frac{Q^*(t)}{\tau} + J_A(t)$$

Table 2.1. *Simplified models of drift zone, in dynamic operation of an IGBT*

2.4. Main IGBT characteristics

The externally measurable relations between the three main parameters in static and quasi-static operations, V_{AK}, I_A, and V_{GK}, are given by the output and transfer characteristics. Figures 2.13a and 2.13b show characteristics of a 1,000 V, 50 A IGBT. As for a power MOSFET output, characteristics show two zones of operation, a saturated zone and a linear zone, separated by a curve which represents the maximum current the IGBT can sustain without any de-saturation (or without channel pinch off). This maximum current is approximately given by the following equation:

$$I_{A\max} = (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK}-V_{th})^2+\frac{2DQ}{W_\nu{}^2}\right]$$

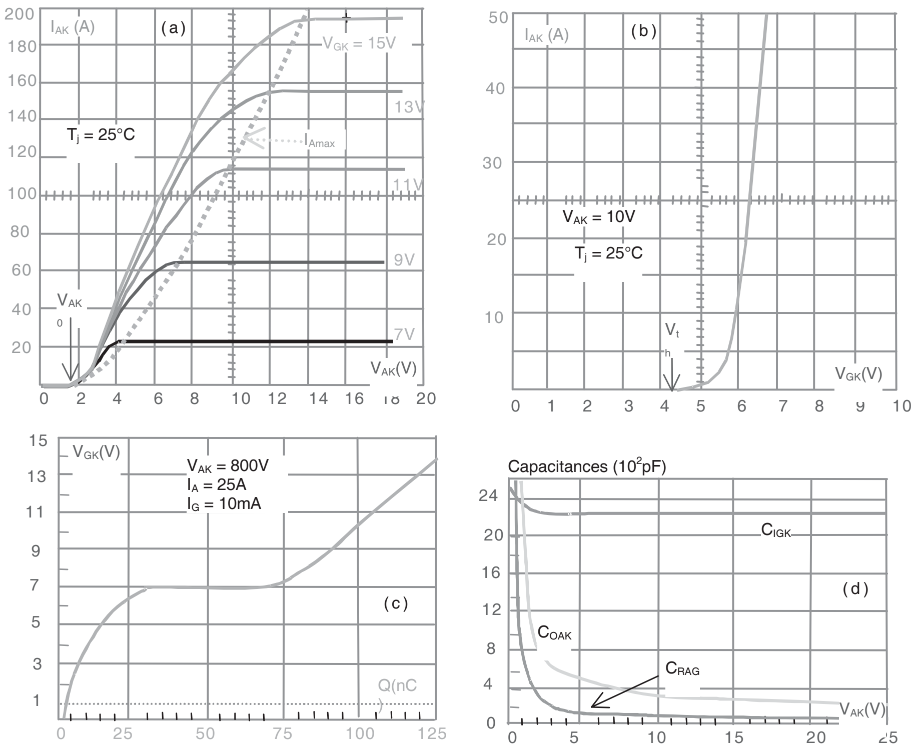


Figure 2.13. *1,000 V, 50 A NPT-IGBT characteristics*

In contrast to the MOSFET I_{Dmax}, the hole current contribution is tied with the bipolar effect. This IGBT output characteristic shows that the voltage drop V_{AK} (around 1V; V_{AK} is the voltage with a quasi-zero current) is larger than that of the MOSFET (around 0V), and larger than that of the bipolar transistor (around 0.2 V), for a 1,000 V device. Voltage drop for this device is around 4 V with a 50 A nominal current, at 25°C. Threshold voltage is V_{th} = 4.5 V, according to the transfer characteristic. Figure 2.13 shows the capacitance characteristics C_{iks}, C_{oks}, C_{rks}, ($C_{ga} = C_{rks}$, $C_{gk} = C_{iks} - C_{rks}$, and $C_{ak} = C_{oks} - C_{rks}$) versus V_{AK} and gate charge. These characteristics are very similar to MOSFET characteristics.

2.5. One cycle of hard switching on the inductive load

Figure 2.14 shows the power circuit and the IGBT simplified model. Parasitic inductive effects in the gate drive and in the power load loop are avoided. Figure 2.15 dipicts the switching waveforms. Compared with the MOSFET current forms, a large difference appears in the anode switch-off current form: instead of quickly going to zero when the anode voltage raises the power supply voltage E, the anode current shows two phases during its fall time: the first is very fast, similar to the MOSFET fall time, and the second is very slow, called the "queue current" or "tail current". Due to the large voltage applied to the IGBT connections at this time, losses due to the "tail" are significant.

The inductive cycle will now be examined phase by phase.

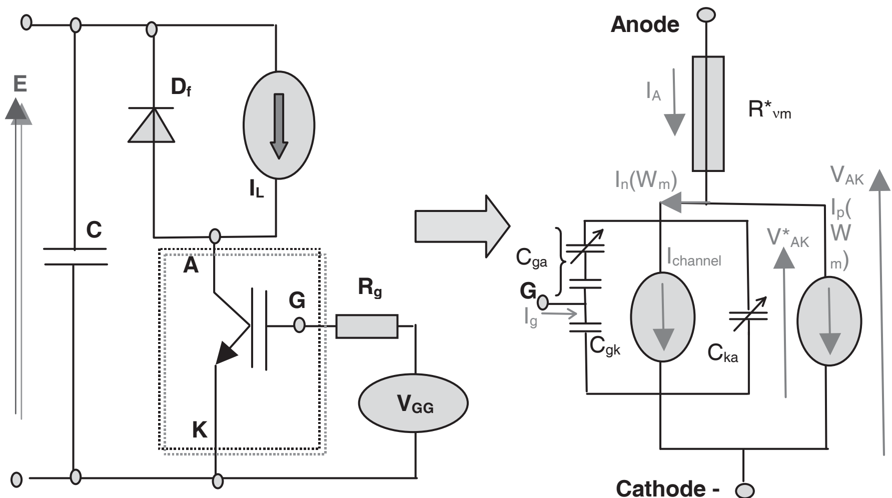


Figure 2.14. *Power circuit and IGBT equivalent circuit during hard switching*

2.5.1. *Switch-on study*

2.5.1.1. *Switch-on delay time $t_{d(on)}$*

Drive voltage rises instantaneously from $-V_{GG}$ to $+V_{GG}$. Gate charge is created according the following equation:

$$V_{GK}(t) = V_{GG}\left[1 - 2e^{-\frac{t}{R_g(C_{gk}+C_{ga})}}\right] \approx V_{GG}\left[1 - 2e^{-\frac{t}{R_g C_{gk}}}\right] < V_{th}$$

This operation is the same in a power MOS: anode current is zero because V_{th} was not yet risen, and the anode voltage is the supply voltage, E.

2.5.1.2. *Current rise time $t_{r(on)}$*

$I_A(t)$ starts when $V_{GK} \geq V_{TH}$, and it increases while the gate is loading. During this phase, the drift zone changes. At the beginning, stored charge quantity is low and the drift zone is divided into three parts, according to Figure 2.16. The first is W_{ZD}, close to the cathode in order to sustain the E voltage. Second is a low level modulated region (W_m), close to the anode. Between these two is an ohmic region, W_R. With the current rise time $I_A(t)$, the stored charge quantity, Q(t), increases, and therefore the low level modulated region becomes a high level region. Also, it expands, and the ohmic region disappears. This phenomenon is complex and will be ignored here. We suppose that, from the starting phase, the drift region is divided into a high-level modulated part, and a space charge part. Space charge distribution is also assumed to be linear. Thus, the increase of anode current is given by the following expression:

$$I_A(t) = (1 + \frac{1}{b})\left[\frac{K_p}{2}(V_{GK}(t) - V_{th})^2 + \frac{2DQ(t)}{W_m(t)^2}\right]$$

where the charge accumulation, neglecting recombination, is given by:

$$\frac{dQ(t)}{dt} = I_{Channel}(t) - [1 - \gamma_p(t)]I_A(t)$$

and I_{AK} increases up to the external limit: $I_L + I_{RM}$.

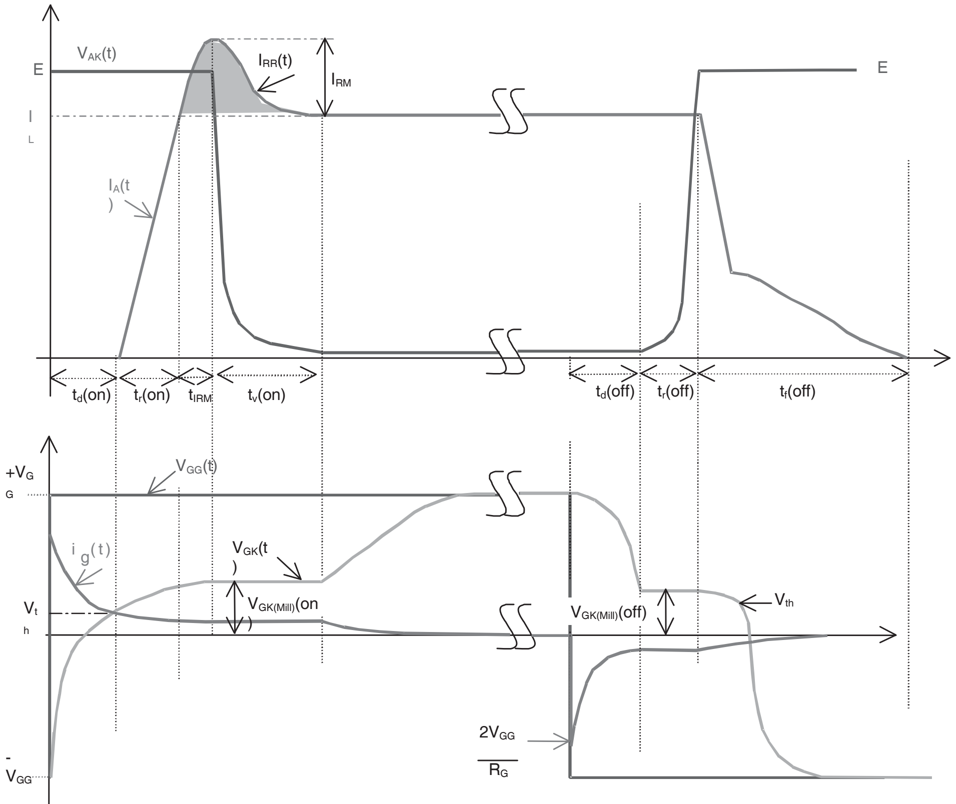


Figure 2.15. *Switching waveforms with inductive load*

2.5.1.3. *Fall time voltage* $t_{v(on)}$

When $I_{AK}(t) = I_L + I_{RM}$, V_{AK} could fall, however, C_{GK} discharges, tied to $dV_{AK}(t)/dt$, and V_{AK} is quasi-constant and is equal to Miller voltage $V_{AK(Miller)on}$. Miller voltage is given by the following expression:

$$I_L + I_{RM} = (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK(Miller)on} - V_{th})^2 + \frac{2DQ}{W_m{}^2}\right]$$

$V_{AK}(t)$ fall time is defined, neglecting the voltage drop in the modulated region, however, the displacing current, tied to the quick change of the boundary between modulated and space charge regions, is taken into account:

$$\frac{dV_{AK}(t)}{dt} = \frac{I_L + I_{RR} - (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK} - V_{th})^2 + \frac{2QD}{W_m^{\ 2}}\right] + (1+\frac{1}{b})\frac{C_{ga}}{C_{ga}+C_{gk}} i_g}{(1+\frac{1}{b})\left[C_{ak} + \frac{C_{gk}C_{ga}}{C_{ga}+C_{gk}} + \frac{C_{ZD}}{3}\cdot\frac{Q}{Q_{Bm}}\right]}$$

$$C_{ZD} = S_{Si}\sqrt{\frac{q\varepsilon_{Si}N_D}{2V_{AK}}} \qquad \text{and} \qquad Q_{Bm} = qN_D W_m S_{Si}$$

As with MOSFETs, we can see a fast fall time at the beginning, and slower fall time as $V_{AK}(t)$ decreases. Stored charges increase according to the equation:

$$\frac{dQ(t)}{dt} = I_{Channel}(t) - (1-\gamma_p)\cdot\left[I_L + I_{RR}\right]$$

However, the increase is negligible while time $t_{v(on)}$ is generally very short. Current $I_{AK}(t)$ during this entire phase is defined by the external current $I_A = I_L + I_{RM}$. When $dV_{AK}/dt = 0$, $V_{GK}(t)$ increases up to V_{GG}, according to the following expression:

$$V_{GK}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gk}+C_{ga})}} - 1\right] > V_{GK(Miller)on}$$

2.5.2. *Switch-off study*

2.5.2.1. *Switch-off delay time $t_{d(off)}$*

The gate drive voltage decreases instantaneously from $+V_{GG}$ down to $-V_{GG}$. Gate voltage discharge is given by:

$$V_{GK}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gk}+C_{ga})}} - 1\right] > V_{GK(Miller)off} > V_{th}$$

IGBT voltage slightly increases until gate voltage V_{GK} is higher than switch-off Miller voltage $V_{GK(Miller)off}$ according to:

$$I_L = (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK(Miller)off} - V_{th})^2 + \frac{2DQ}{W_\nu^{\ 2}}\right]$$

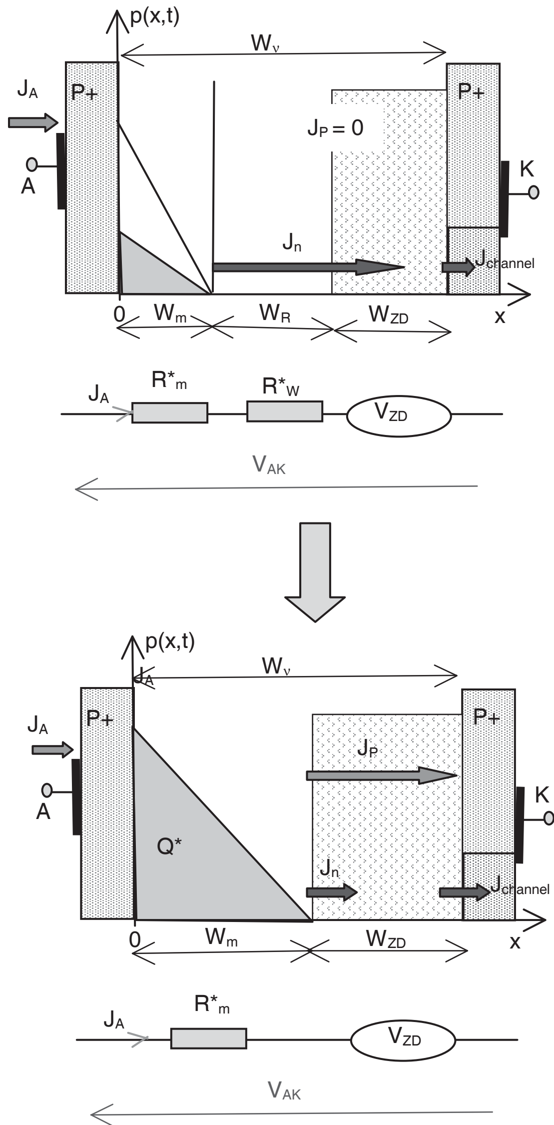


Figure 2.16. *Drift zone evolution during the anode current rising time*

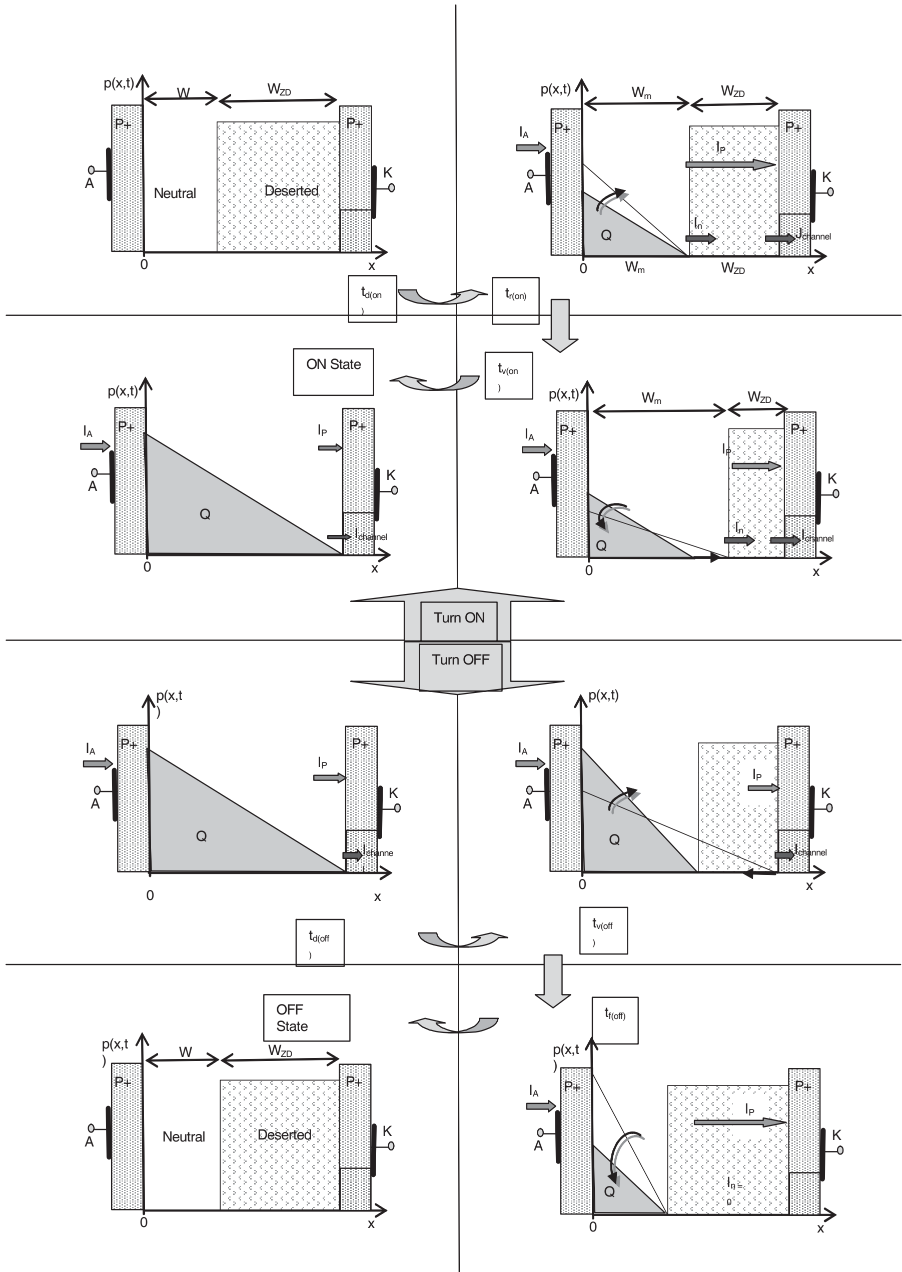


Figure 2.17. *Charge evolution in the drift zone during one switching cycle on an inductive load*

I_{AK} is still forced to equalize the load current, I_L, and the voltage V_{AK} is under the same law that applied in the on-phase. Channel current (electrons) decreases because the gate voltage decreases, and the process of charge storage slows down. Stored charge also decreases if the delay is large (high R_G). The quantity of charge is determined by the following equation:

$$\frac{dQ(t)}{dt} = -\frac{Q}{\tau} + I_{Channel}(t) - (1-\gamma_p)I_L$$

2.5.2.2. *Voltage rise time $t_{v(off)}$*

When the gate voltage V_{GK} is equal to the Miller voltage $V_{GK(Miller)off}$, V_{AK} starts to rise. The gate voltage is constant and equal to $V_{GK(Miller)off}$, because capacitance C_{GA} is charged by the current allowed by $dV_{AK}(t)/dt$. Speed is given by:

$$\frac{dV_{AK}(t)}{dt} = \frac{I_L - (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK} - V_{th})^2 + \frac{2QD}{W_m^{\ 2}}\right] + (1+\frac{1}{b})\frac{C_{ga}}{C_{ga}+C_{gk}} i_g}{(1+\frac{1}{b})\left[C_{ak} + \frac{C_{ge}C_{gc}}{C_{ga}+C_{gk}} + \frac{C_{ZD}}{3}\cdot\frac{Q}{Q_{Bm}}\right]}$$

As with MOSFETs, and for the same reasons, voltage rise starts slowly then increases speed. Current I_{AK} is still equal to I_L during this phase, and the charge quantity follows the aforementioned law. $t_{v(off)}$ is generally short and the stored charge variation can be neglected.

2.5.2.3. *Current fall time $t_{f(off)}$*

When V_{AK} raises the supply voltage, E, Miller effect disappears with $dV_{AK}(t)$ / = 0. Gate voltage can now decrease according to the equation:

$$V_{GK}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{ga}+C_{ga})}} - 1\right] \approx V_{GG}\left[2e^{-\frac{t}{R_g C_{gk}}} - 1\right] > V_{th}$$

Anode current can also decrease: fast decrease also occurs with power MOSFET and follows the gate voltage discharge, then a “tail” starts when the channel is opened ($V_{AK}(t)<V_{th}$). As the tail is slow, we can admit that: $t_{f(off)} = t_{tail}$. The tail value

and its duration depends on the stored charge and the recombination rate. It may be estimated as:

$$I_A(t) = I_{tail}(t) = (1+\frac{1}{b})\frac{2DQ(t)}{W_m{}^2} \qquad \text{with} \qquad W_m = W_v - \sqrt{\frac{2\varepsilon_{Si}E}{qN_D}}$$

Charges mainly disappear by recombination, but electron injection into the P+ anode (reverse injection) speeds up the process. Thus:

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} - (1-\gamma_p)I_A(t)$$

According to this equation, the reverse injection of electrons in the P+ anode is equivalent to a stored charge extraction, and its effect is stronger when the P+N- injection coefficient is smaller. This phase ends when stored charges in the drift zone are close to zero.

If the stored charge is assumed to be linear, Figure 2.17 shows qualitatively the charge evolution in the drift zone, on inductive load, during the entire switching cycle.

Table 2.2 lists the various external parameters variations.

From the previous analysis, we can see that a high speed of the gate drive allows a decrease of switching times and an increase of $dI_A(t)/dt$ and $dV_{AK}(t)/dt$, during switch-on and switch-off. Accordingly, its allows for a reduction of losses.

SWITCH-ON				
$t_{d(on)}$	$V_{ak}(t)=E$	$I_A(t)=0$	$V_{GK}(t)=V_{GG}\left[1-2e^{-\frac{t}{R_g(C_{gk}+C_{ga})}}\right]\approx V_{GG}\left[1-2e^{-\frac{t}{R_gC_{gk}}}\right]<V_{th}$	$Q(t)=0$
$t_{r(on)}$	$V_{AK}(t)=E$	$I_A(t)=(1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK}(t)-V_{th})^2+\frac{2DQ(t)}{W_m(t)^2}\right]$	$V_{GK}(t)=V_{GG}\left[1-2e^{-\frac{t}{R_g(C_{gk}+C_{ga})}}\right]\approx V_{GG}\left[1-2e^{-\frac{t}{R_gC_{gk}}}\right]>V_{th}$	$\frac{dQ(t)}{dt}=I_{Channel}(t)-(1-\gamma_p)I_A(t)$
$t_{V(on)}$	$\frac{dV_{AK}(t)}{dt}=\frac{I_L+I_{RR}-(1+\frac{1}{b})\left[I_{An}-\frac{C_{ga}}{C_{ga}+C_{gk}}i_g\right]}{(1+\frac{1}{b})\left[C_{ak}+\frac{C_{gk}C_{ga}}{C_{ga}+C_{gk}}+\frac{C_{ZD}}{3}\cdot\frac{Q}{Q_{Bm}}\right]}$ $I_L=\frac{K_p}{2}(V_{GK}-V_{th})^2+\frac{2QD}{W_m{}^2}$	$I_A=I_L+I_{RR}$	$V_{GK}=V_{GK(Miller)on}$	$\frac{dQ(t)}{dt}=I_{Channel}(t)-(1-\gamma_p)(I_L+I_{RR})$
ON-STATE				
	$V_{AK}=V_{P^+N^-}+I_L\cdot(R_{vm}+R_{Channel})$	$I_A=I_L$	$V_{GK}=+V_{GG}$	$Q=(\gamma_p-\frac{\beta_{PNP}}{1+\beta_{PNP}})\cdot I_L\cdot\tau$
SWITCH-OFF				
$t_{V(off)}$	$\frac{dV_{AK}(t)}{dt}=\frac{I_L-(1+\frac{1}{b})\left[I_L-\frac{C_{ga}}{C_{ga}+C_{gk}}i_g\right]}{(1+\frac{1}{b})\left[C_{ak}+\frac{C_{gk}C_{ga}}{C_{ga}+C_{gk}}+\frac{C_{ZD}}{3}\cdot\frac{Q}{Q_{Bm}}\right]}$ $I_L=\frac{K_p}{2}(V_{GK}-V_{th})^2+\frac{2QD}{W_m{}^2}$	$I_A(t)=I_L$	$V_{GK}=V_{GK(Miller)off}$	$\frac{dQ(t)}{dt}=-\frac{Q}{\tau}+I_{Channel}(t)-(1-\gamma_p)I_L$

$t_{f(off)}$	$V_{AK}(t) = E$	$I_A(t) = (1+\frac{1}{b})\frac{2DQ}{W_m^2}$	$V_{GK}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gk}+C_{gk})}} - 1\right] < V_{th}$	$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} -(1-\gamma_p)I_L(t)$
OFF-STATE				
	$V_{AK}(t) = E$	$I_A(t) = 0$	$V_{GK}(t) = -V_{GG}$	$Q = 0$

Table 2.2. E*volution of external quantities during one switching cycle on an inductive load*

A power load circuit has various effects that differ at switch-on and switch-off. Table 2.3 gives a qualitative evaluation. Figure 2.18 shows application results from a 1,000 V, 50 A PT-IGBT, with the same drive and test temperature. We can see that voltage E only has an effect on stored charge, after the current's initial rising phase.

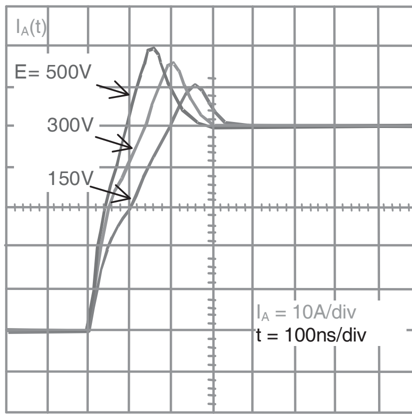
The duration of the Miller "plateau", at switch-on and switch-off, depends on R_g: it is short when R_g is small. When the drive is fast and current i_g is larger than the charge and discharge currents given by $dV_{AK}(t)/dt$, the Miller effect disappears. In this case, $dV_{AK}(t)/dt$ is the same, but V_{GK} voltage is no longer constant during $t_{v(on)}$ and $t_{v(off)}$, and is given by the equation:

$$(C_{gk} + C_{ga})\frac{dV_{GK}}{dt} = C_{ga}\frac{dV_{AK}}{dt} + i_g$$

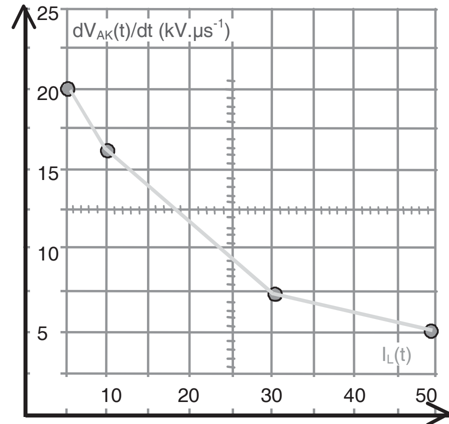
$$V_{GG} = R_g i_g + V_{GK}$$

POWER	SWITCH ON			SWITCH OFF		
	$dI_A(t)/dt$	$dV_{AK}(t)/dt$	$V_{GK(Miller)on}$	$I_{tail}(t)$	$dV_{AK}(t)/dt$	$V_{GK(Miller)off}$
E ↗(W_m ↘)	↗	(↗)		↗	(↗)	
I_L ↗	(↗)	↘	↗	(↗)	↗	↗
I_{RR} ↗		↘	↗			

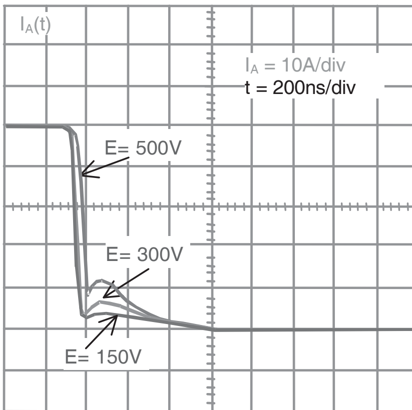
Table 2.3. *Power load effects on IGBT, during hard switching operation*



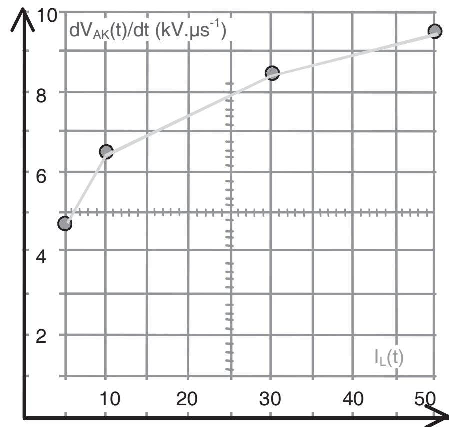
(a)



(b)



(c)



(d)

Figure 2.18. *Load effects on IGBT behavior in hard switching: a) and b) switch-on; c) and d) switch-off*

2.6. Soft switching study

2.6.1. *Soft switching switch-on: ZVS (Zero Voltage Switching)*

ZVS operation is performed during an interval at zero current and quasi-zero voltage, before connection of the power load. This interval depends on the application: Figure 2.19 shows the phases of an application, together with the associated waveforms. The ZVS target is to apply I_{load} with a low voltage V_{AKmax} and within a minimum of time $t_v(_{ZV})$, in other words with a minimal dynamic voltage. Two conditions are applied on the gate drive. First, gate voltage $V_{GG}(t)$ must occur at a sufficient time $t_{pre}(on)$ before the current application, in order to obtain a V_{GK} voltage higher than V_{th} before application of the load current. Second, the speed of increase of the gate voltage $V_{GK}(t)$ must be high enough in order to obtain a channel current greater than the applied current: $dI_{channel}(t)/dt > dI_L(t)/dt$. This operation is called "switch-on preconditioning". If this condition is not realized, a desaturation phenomenon appears, and V_{AKmax} could raise the supply voltage. With the correct preconditioning operation, the drift zone may be roughly represented by two sub-regions: one a high modulated level, W_m, and a neutral ohmic one, W_R (see Figure 2.19b). Thus, the anode to cathode voltage is approximately:

$$V_{AK}(t) = V_{P^+N^-}(t) + I_A(t) \cdot [R_m(t) + R_w(t) + R_{Channel}(t)]$$

Neglecting re-combinations, storage charges follow the law:

$$Q(t) = \int_0^t I_A(t)dt$$

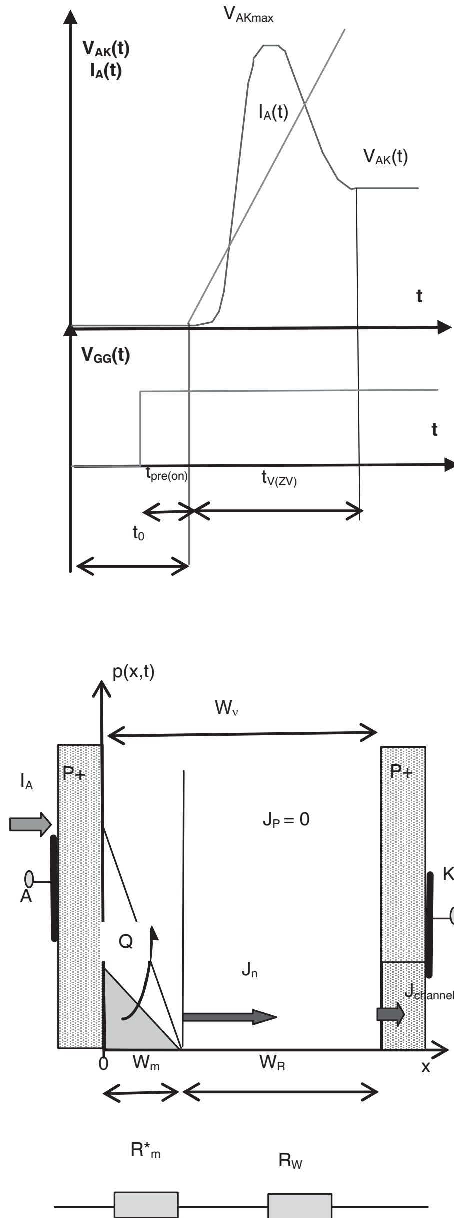


Figure 2.19. *Soft switching (ZVS): a) waveforms; b) charge evolution*

In order to obtain a reliable dynamic voltage, charges must be stored quickly. However, the available stored charge for a given load current is accordingly weak when the current speed is too fast. As a result, $V_{AK}(t)$, the soft switching dynamic voltage in ZVS during time $t_v(_{ZV})$, is highly significant when $dI_L(t)/dt$ is high. This phenomenon is the same as in bipolar diodes during switch-on. Compared to bipolar transistors, the IGBT dynamic voltage is much lower, because the charge storage made by the $I_L(t)$ current is faster than the storage made by the $I_b(t)$ current, except when the base current is higher than the I_L current in amplitude and speed. Figure 2.20 shows experimental results with a PT-IGBT, which confirm the weak IGBT dynamic voltage in ZVS operation.

2.6.2. *Soft switching switch-off: ZCS (Zero Current Switching)*

Here, two switching modes are distinguished: thyristor and thyristor-diode modes. The first mode occurs when an IGBT and anti-paralleled diode are series connected with a diode. The latter is omitted in the thyristor-diode mode. During operation, the thyristor-diode mode is characterized by a reverse current applied on the switch, while in the thyristor mode, this current is stopped by the series connected diode.

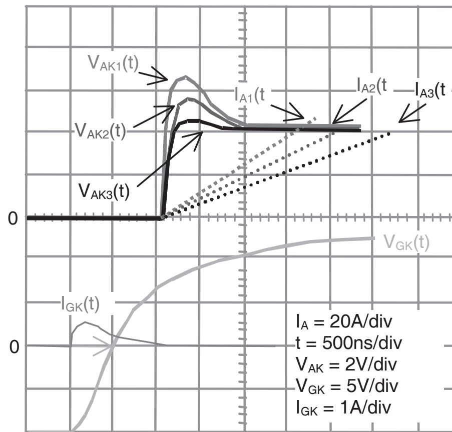


Figure 2.20. *1,000 V, 50 A PT-IGBT with ZVS*

Figure 2.21 shows various switching phases and associated waveforms for a ZCS thyristor mode operation. The IGBT anode current is cancelled by the power load current action at t = 0, and it remains zero while the V_{AK} voltage is quasi-zero, during a time t_c (it is slightly negative due to anti-paralleled diode forward voltage,

V_F). This interval is fully dependent on the power load. At the completion of t_c time, a positive voltage $V_{AK}(t)$ is applied to the switch, and IGBT terminals. At this time, a switch-on current appears, caused by the remaining stored charges in the IGBT. Soft switching in thyristor mode minimizes this current, when the load voltage appears. Switch-off of the gate drive voltage must occur before this load voltage, with a minimum advance $t_{pre(off)min}$, giving enough time to the gate drive to be under the threshold voltage V_{th}. This process is called "switch-off preconditioning drive".

At time t = 0, the conduction stored charges are in the drift zone, even if the anode current becomes zero. During t_c, Q_o is reduced using two methods: recombination, which is the main mechanism, and internal diffusion currents, which may occur only if the channel is still conducting. Thus:

$$\frac{dQ(t)}{dt} = -\frac{Q}{\tau} + qD\left.\frac{dp(x,t)}{dx}\right|_{x=W_v}$$

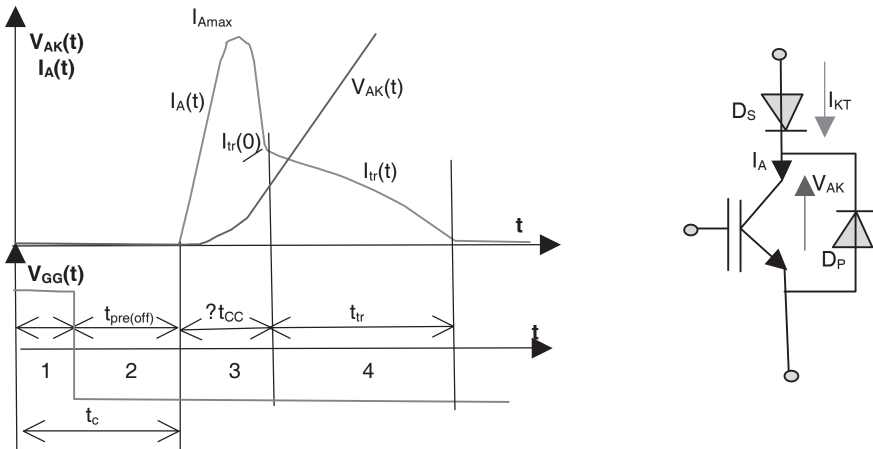


Figure 2.21. *ZCS in thyristor mode*

At t = t_c, $V_{AK}(t)$ is applied, and the channel is opened by the preconditioning, but some stored charge remains in the drift zone. IGBT is not able to sustain the imposed load voltage, so, the charge concentration at x = W_v, $p(W_v)$, is not zero. Therefore, a short circuit appears, through the IGBT and the inductive connections L_{conn}, on the applied voltage $V_{ap}(t)$, until the storage charge cancellation at x =W_v, $p(W_v) = 0$. Short circuit current (peak current) is given by the equation:

$$I_{A\max} = \frac{1}{L_{conn}} \int_{t_c}^{t_c+\Delta t_{sc}} \left[V_{ap}(t) - V_{AK}(t) \right] dt$$

This short circuit phase is longer when the stored charge at t = t_c is greater.

At the end of this phase, IGBT recovers its power to sustain a positive voltage, even if some remaining charges are still in the drift zone. So, a tail can appear, as with hard switching, but the applied voltage is now variable. This tail with variable applied voltage is:

$$I_A(t) = (1+\frac{1}{b})\frac{2DQ(t)}{W_m{}^2} \quad , \quad \frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} - (1-\gamma_p)I_A(t)$$

$$W_m = W_v - \sqrt{\frac{2\varepsilon_{Si} V_{AK}(t)}{qN_D}}$$

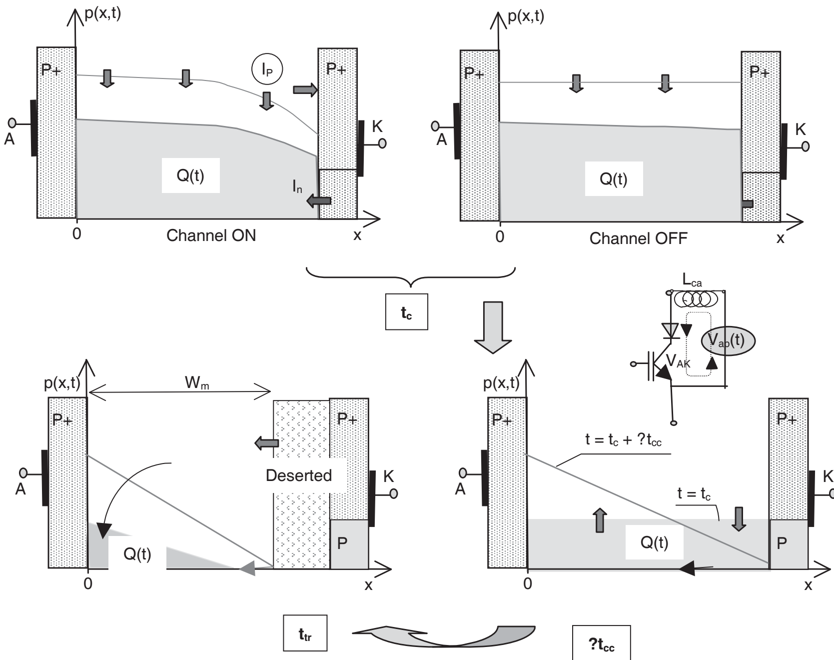


Figure 2.22. *Charge evolution in ZCS thyristor mode*

Figure 2.22 depicts charge evolution during the various ZCS phases, in the thyristor mode. The following is a list of the main switching parameters mentioned in the previous analysis:

– *The recombination time* t_c: the stored charge is lower when this time is long. But it is tied to the application constrains, mainly the working frequency.

– *The preconditioning time* $t_{pre(off)}$: in order to have diffusion currents, when the external current equals zero, this time must be as small as possible. In other words, the channel must be on for as long as possible.

– *The applied voltage speed* $dV_{AK}(t)/dt$: a low speed allows a small turn on current, but it is entirely tied to the application.

Figure 2.23 shows the experimental results supporting these statements. The short circuit makes few losses, even with a high peak current. The tail makes the majority of losses.

Figure 2.24a shows the various switching phases with the corresponding waveforms in the thyristor-diode mode. Some differences occur during the recombination phase t_c, and on the external voltage application, according to the thyristor mode waveforms. During t_c, instead of a zero current in a thyristor-diode mode operation, an inverse current, due to the power load, is applied to the IGBT and the anti-parallel diode. Conversely, the applied voltage shows a steep gradient, followed by a constant voltage, like in hard switching operation.

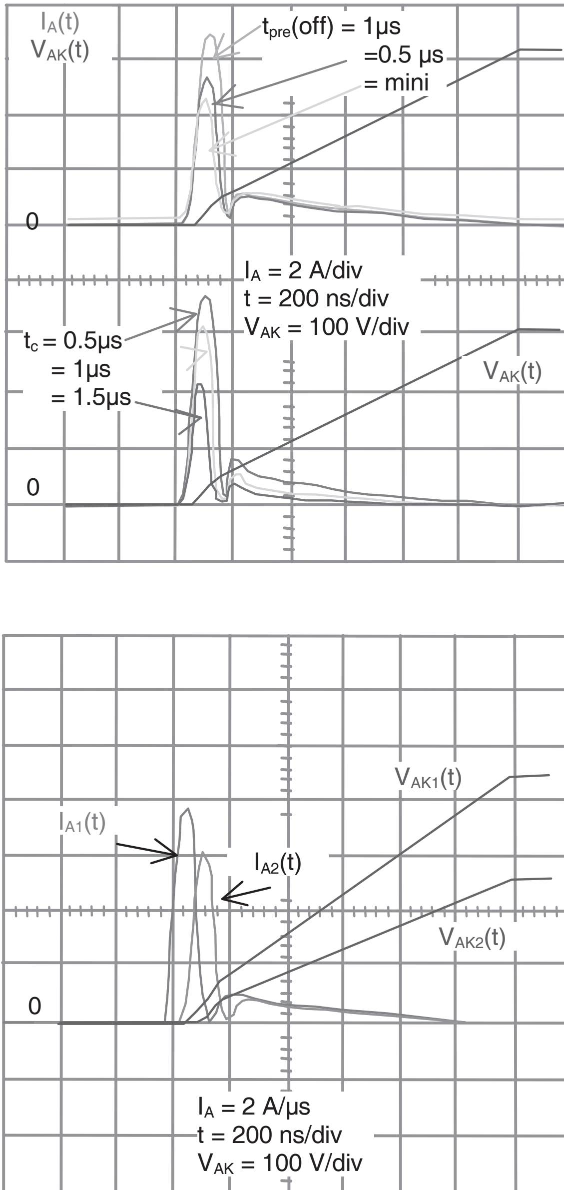


Figure 2.23. *PT-IGBT 1,000 V, 50 A in ZCS thyristor–mode, versus,* $t_{pre(off)}$, t_c, $dV_{AK}(t)/dt$

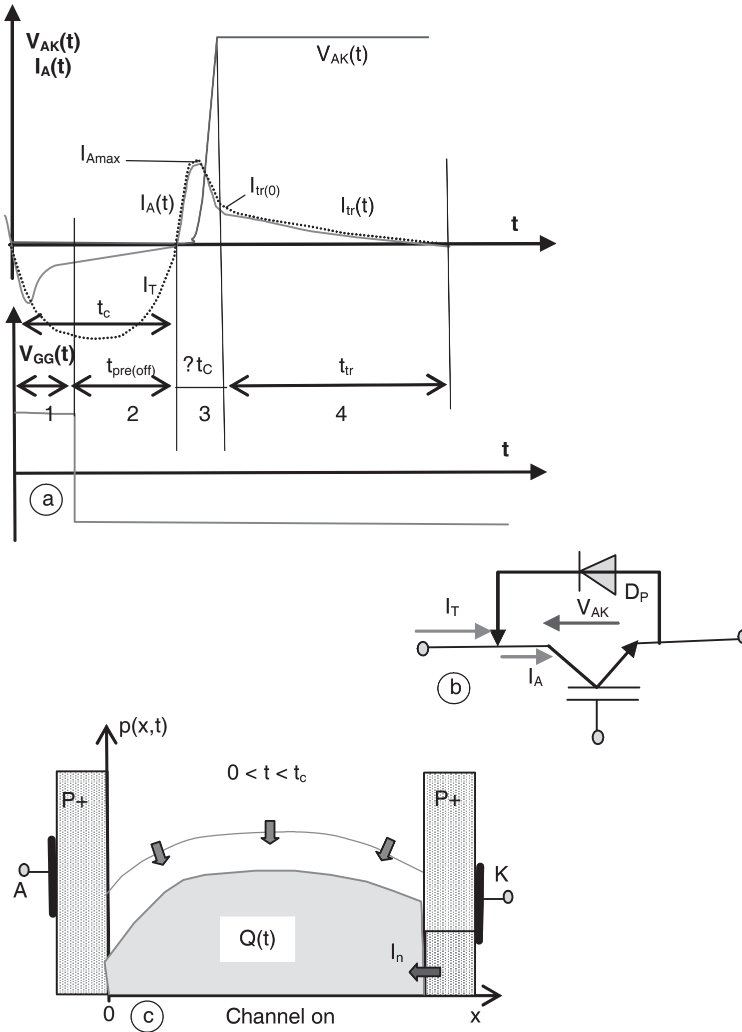


Figure 2.24. *ZCS soft switching in thyristor–mode operation*

The inverse current is split between the anti-parallel diode and the IGBT. Due to the low reverse voltage made by the diode, the IGBT forward voltage is able to take only a very small part of this current. Accordingly, the extraction of stored charge is weak. Nevertheless, it is possible to use this low reverse current to extract a maximum stored charge: during the reverse conduction, the channel may be opened; or in on-state, according to the drive applied. If the channel is opened, the reverse conduction is only made by the PNP bipolar transistor under the effect of the stored

charge effect. Thus, charge extraction is impossible, while the reverse current is comprised solely of hole charges. Now, if the channel is on, electrons create the reverse current from the channel, while the hole current is driven by the anode. Stored charge disappears by recombination, reverse current extraction and internal diffusion current (see Figure 2.24c).

$$\frac{dQ(t)}{dt} = -\frac{Q}{\tau} + qD\frac{dp(x,t)}{dx}\bigg|_{x=W_v} - I_{Treverse}$$

Figure 2.25 shows the extraction effect made by the on-channel in 1,000 V, 25 A NPT-IGBT. As for the thyristor mode operation, it is necessary to reduce the preconditioning time in order to obtain a maximum extraction. The short circuit phase is the same as in the thyristor mode operation, and the tail is equivalent to the one made by the hard switching operation.

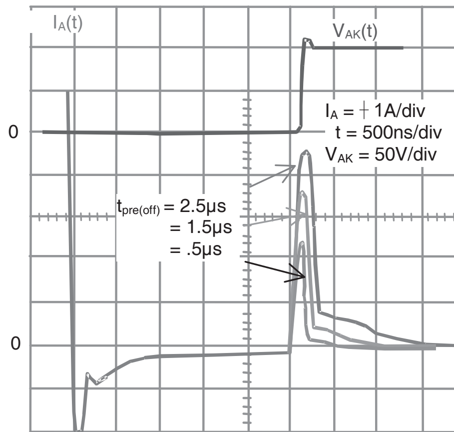


Figure 2.25. *1,000 V, 50 A NPT-IGBT in ZCS-thyristor-diode, versus* $t_{pre(off)}$

2.7. Temperature operation

Neglecting second order effects, the IGBT overall voltage drop is the sum of three parameters: the V_{P+N-} junction potential, the modulated drift zone drop voltage, and the channel voltage drop. Two resistors, R_{vm} and $R_{channel}$, could represent the two last parameters. The V_{P+N-} potential at zero current is the V_{AK0} voltage drop. It increases with the charge concentration p(0); and has a negative temperature coefficient. The channel resistance has a positive temperature coefficient, thanks to

the reduction of electron surface mobility. R_{vm} temperature coefficient depends on μ_n and Q, two terms which have two opposite temperature coefficients. Versus temperature, electron bulk mobility μ_n decreases while quantity of charges Q increases, due to an increase of the carriers lifetime. This last one and the recombination rate varies according to the following law:

$$\tau(T_j) = \tau(T_{j0})\left[\frac{T_j}{T_{j0}}\right]^{\alpha_\tau}$$

where T is in Kelvin.

The exponential coefficient α_τ is positive and higher when the lifetime is shorter. If the quantity of stored charges Q varies with the same law (this assumption is not really verified because it could be necessary to consider the injection coefficients of injectors with temperature), the μ_n.Q term variation versus temperature is:

$$\mu_n(T_j)Q(T_j) = \mu_n(T_{j0})Q(T_{j0})\left[\frac{T_j}{T_{j0}}\right]^{(\alpha_\tau - 2,5)}$$

The temperature coefficient of R_{vm} is positive for $\alpha_\tau < 2.5$ and negative for $\alpha_\tau > 2.5$.

In conclusion it would be seen that the global forward voltage versus temperature is quite complex, depending on each factor of the whole voltage, and on their appropriate coefficients versus temperature. Thus depending on the technological production process.

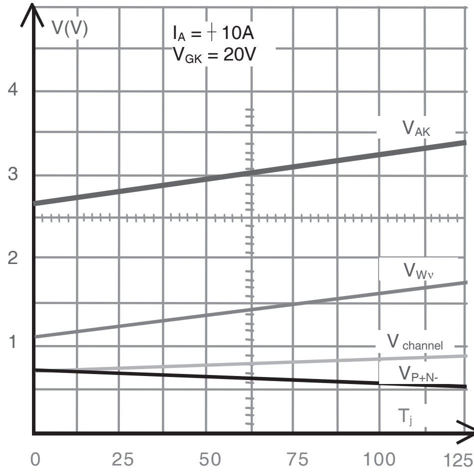


Figure 2.26. *1,000 V, 10 A PT-IGBT: three voltage distributions versus temperature*

Figure 2.26 shows an example of three voltage variations versus temperature.

The NPT-IGBT includes a large drift zone and a long carrier lifetime. If the carrier lifetime is in the region of $\alpha_\tau << 2.5$, the $R_{\nu m}$ resistance temperature coefficient is positive. This way, two terms have a positive temperature coefficient: $R_{\nu m}$ and $R_{channel}$, and one term has a negative temperature coefficient: V_{P+N-}. As a result, their global temperature coefficient is positive.

Now, the PT-IGBT has a very low carrier lifetime, giving a large value for α_τ. Their $R_{\nu m}$ temperature coefficient is rather negative. So now, two parameters have a negative temperature coefficient: $R_{\nu m}$ and V_{P+N-}, while one term has a positive temperature coefficient: $R_{channel}$. Therefore, the PT-IGBT has a negative temperature coefficient.

The anode current I_A also has an influence on the forward voltage temperature coefficient. With a very low current, voltage drops in $R_{\nu m}$ and $R_{channel}$ are small compared to those in V_{P+N-} (close to V_{AK0}). Thus, the temperature coefficient is negative, whatever the technology, PT or NPT. When I_A increases, the voltage drops in $R_{\nu m}$ and $R_{channel}$ increase, and the whole temperature coefficient may be positive or negative, according to the $R_{\nu m}$ temperature coefficient. With a large current, the part tied to the channel, $R_{channel}$, is preponderant and the temperature coefficient is positive whatever the technology. Figure 2.27 shows static characteristics I_A, V_{AK} at 25°C and 125°C, for a 1,200 V, 150 A NPT-IGBT, and a 1,200 V, 100 A PT-IGBT.

Charge recombination rates are respectively 20 µs and 0.4 µs. We can see that the 25°C and 125°C curves cross, whatever the technology. However, the cross point is located at very low current for the NPT-IGBT, and at a higher current level for the PT-IGBT.

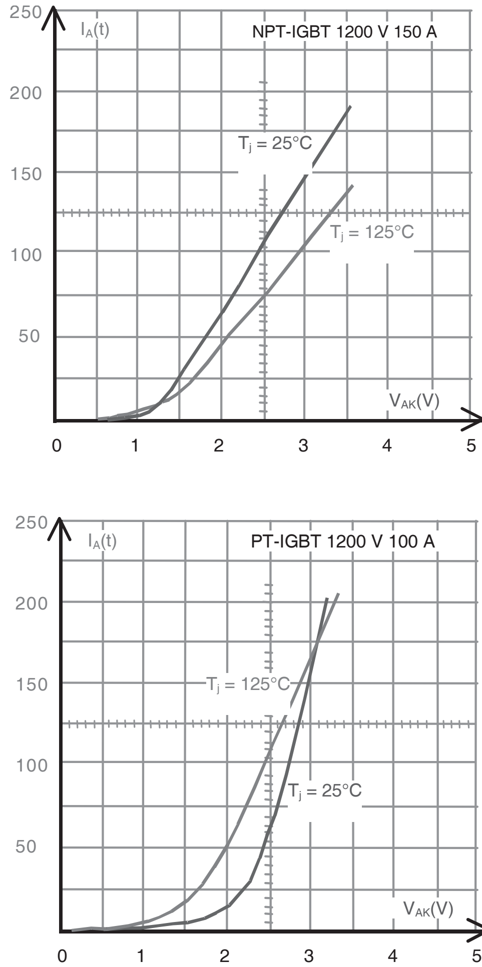


Figure 2.27. *I_A, V_{AK} characteristics versus temperature*

Temperature makes a stored charge increase and a channel conductivity decrease, so the overall IGBT switching performances are worse when temperature increases. For the hard switching operation, the switch-on and switch-off speeds, $dI_A(t)/dt$ and $dV_{AK}(t)/dt$, are reduced and the tail current is seriously enlarged (see

Figure 2.28a and b). For the soft switching operation, the increase of temperature damages the dynamic voltage (ZVS), increases the re-starting current (ZCS), and so makes an increase of switching losses (see Figure 2.28c and d).

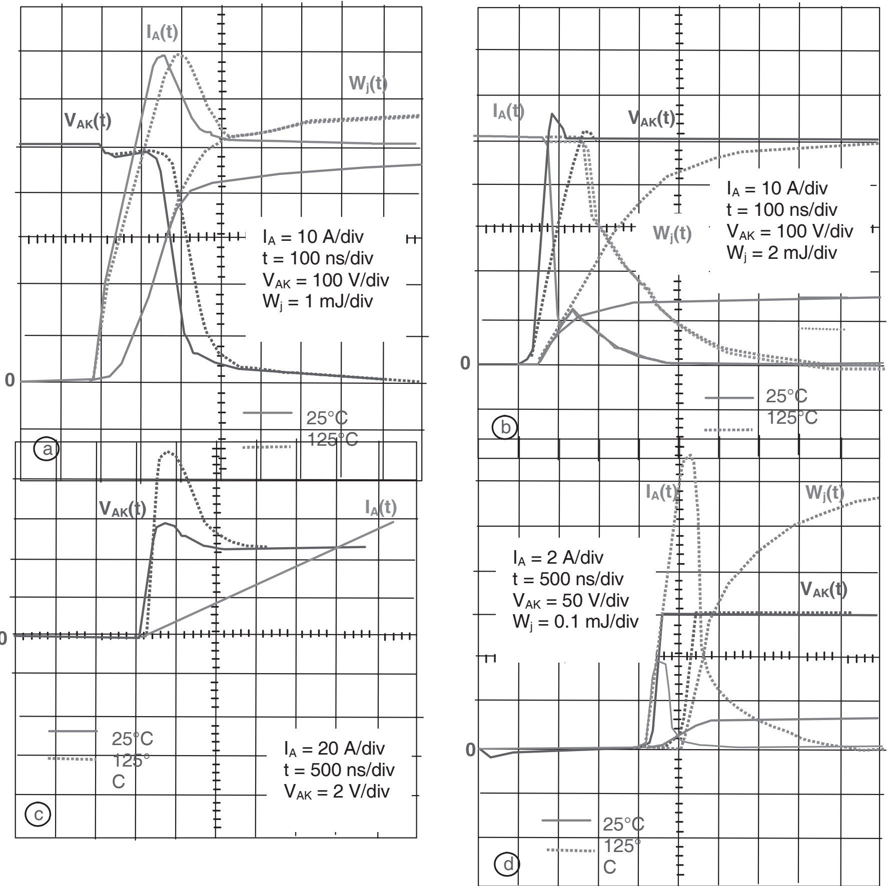


Figure 2.28. *a) Hard switching turn-on, b) hard switching turn-off, c) ZVS turn-on d) ZCS turn-off*

2.8. Over-constraint operations

2.8.1. *Overvoltage*

Overvoltages may occur on gate or anode. Channel structure for MOSFET or IGBT is the same, so the remarks made for the MOSFET in over-constrained

regimes are the same. Anode-cathode avalanche sustaining voltage is less for IGBT than for MOSFET, due to the internal PNP. Even if the IGBT are specificed as sustaining an avalanche voltage, of lower magnitude than the MOSFET, it is advised to use an avalanche protection between anode and cathode for a longer lifetime. While the NPT-IGBT has a thick drift zone, and while the PNP bipolar transistor is weaker than that in the PT technology, this NPT technology is better in terms of sustaining an avalanche.

2.8.2. *Over-current*

If the mounting procedure is sound, two phenomenons roughly limit the anode current density in the transient regime of an IGBT: the parasitic thyristor switch-on, and the N- drift zone avalanching at high current density (also called dynamic avalanche). The parasitic thyristor turns on when:

$$J_{A\max(Thy)} < (1+\frac{1}{\beta_{PNP}})\cdot\frac{0.6}{R_P \cdot S_{Si}}$$

Resistance R_p (according to Figure 2.29) is given by:

$$R_P = \frac{L_P}{H \cdot Z}\cdot\frac{1}{q\mu_p N_A}$$

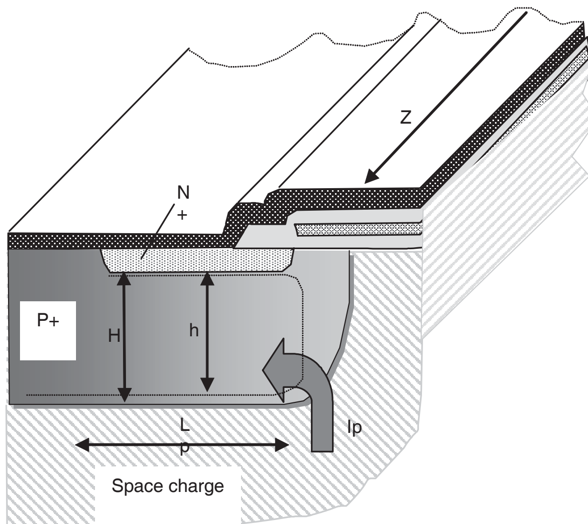


Figure 2.29. *R_p in the Pwell, with a hole current*

For a Pwell defined by L_p = 6 µm, N_A = 10^{17} cm^{-3}, H = 10 µm, μ_p = 300 $cm^2.V^{-1}.s^{-1}$, Z = 5m per square centimeter of silicon, resistance R_p is equal to 0.25 mΩ. The theoretical density $J_{Amax(thy)}$ achieved is 9.6 kA.cm^{-2} and 4.8 kA.cm^{-2} respectively, for a β_{PNP} of 0.3 or 1 we can see that these values are very large.

$J_{Amax(thy)}$ is also linked to the operation conditions. Due to the space charge extension in the P region of the Pwell when the applied voltage on the anode increases, the way through for holes shrinks, causing a $J_{Amax(thy)}$ reduction. This effect is not important, due to the great dissymmetry in the doping levels N_A and N_D. For example, an anode voltage of 600 V leads to an H-h of 0.1µm. Temperature also has a negative effect on the triggering current density, because it decreases the hole mobility in the Pwell. For example, $J_{Amax(thy)}$ is divided by two when the temperature increases from 25°C to 125°C. Voltage and temperature increase the β_{PNP} gain, which in turn reduces $J_{Amax(thy)}$. As a conclusion, today, the parasitic thyristor of IGBT is no longer a difficulty if the maximum gate voltage is respected.

If an over-current occurs together with a gate overvoltage, the channel current could potentially be high enough to switch the thyristor on. The maximum current versus gate overvoltage (<20 V) assessment is complex. The following expression can approximate the maximum current if a high level modulated region and a space region divide the drift zone:

$$J_{A\max} = (1+\frac{1}{b})\left[\frac{K^*_p}{2}(V_{GK\max} - V_{th})^2 + \frac{2DQ^*_{\max}}{W_{m(\min)}^{\ 2}}\right]$$

where Q^*_{max} and $W_{m(min)}$ represent the maximum stored charge density and the modulated regions minimum thickness.

This equation shows that J_{Amax} is larger when V_{GK} increases. If J_{Amax} is compared to MOSFET J_{Dmax}, equations show the additional hole current in the IGBT. Figure 2.30a shows J_{Amax} versus gate overvoltage, for an experimental example. At high V_{GK}, a saturated behavior occurs for J_{Amax}, under a high electric field, due to electron mobility reduction in the channel. Despite this self limitation, current density J_{Amax} can be very high if the gate overvoltage is excessive, and thus, switch-on of the thyristor could occur, (see Figure 2.30b). Therefore, a gate overvoltage protection must be used.

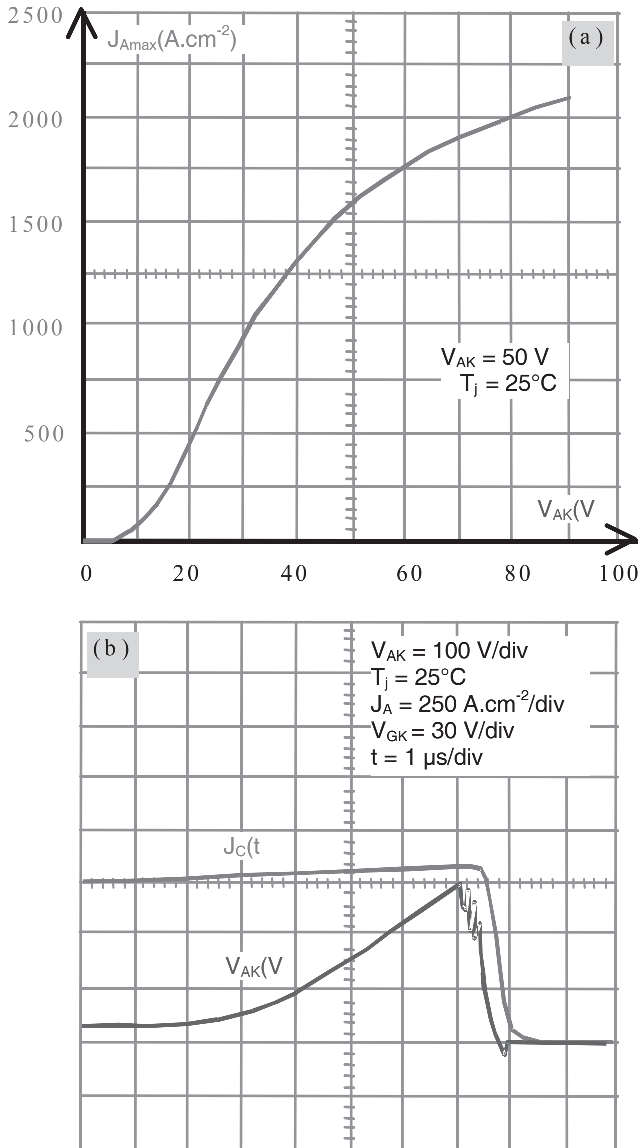


Figure 2.30. *a) Max current density with high gate voltage; b) NPT-IGBT parasitic thyristor switch-on*

With an applied voltage on anode-cathode terminals, an electric field is installed in the drift zone, if it exists, and at the same time a high anode current is applied. The electric field peak can be amplified, and may raise the silicon critical field. At this time, a dynamic avalanche occurs. The following equation ties the electric field and the space charge (see Figure 2.31a):

$$\frac{dE_A(x,t)}{dx} = -\frac{q}{\varepsilon_{si}}[N_D + p(x,t) - n(x,t)] = -\frac{q}{\varepsilon_{si}}[N_D + \frac{1}{qv_n(x,t)} \cdot \frac{K_{PNP}(x,t)\delta(x,t) - 1}{1 + K_{PNP}(x,t)} \cdot J_A]$$

where $\delta(x,t)$ is the ratio between hole and electron speeds $v_n(x,t)/v_p(x,t)$, and $K_{PNP}(x,t)$ is the ratio between hole current and the electron current densities $Jp(x,t)/Jn(x,t)$.

Reasonably, $K_{PNP}(x,t)$ can be exchanged with the PNP bipolar transistor dynamic gain, β_{PNPdyn}, and we can assume that this gain is constant along the space charge. Electron speed is three times higher than the hole speed at a low electric field, but these two speeds are the same ($v_{ns} = v_{ps} = 10^7 cm.s^{-1}$) when the field is higher than 5 $V.\mu m^{-1}$. Then the field E_{Amax} raises the silicon critical field E_{simax}. $E_A(x,t)$ is higher than 5 $V.cm^{-1}$ on a large part of the space charge. Consequently the hypothesis $\delta(x,t) = 1$ on the whole space charge can be considered as acceptable (see Figure 2.31b). Thus, the previous equation becomes:

$$\frac{dE_A(x,t)}{dx} = -\frac{q}{\varepsilon_{si}}[N_D + \frac{1}{qv_{ns}} \cdot \frac{\beta_{PNPdyn} - 1}{1 + \beta_{PNPdyn}} \cdot J_A]$$

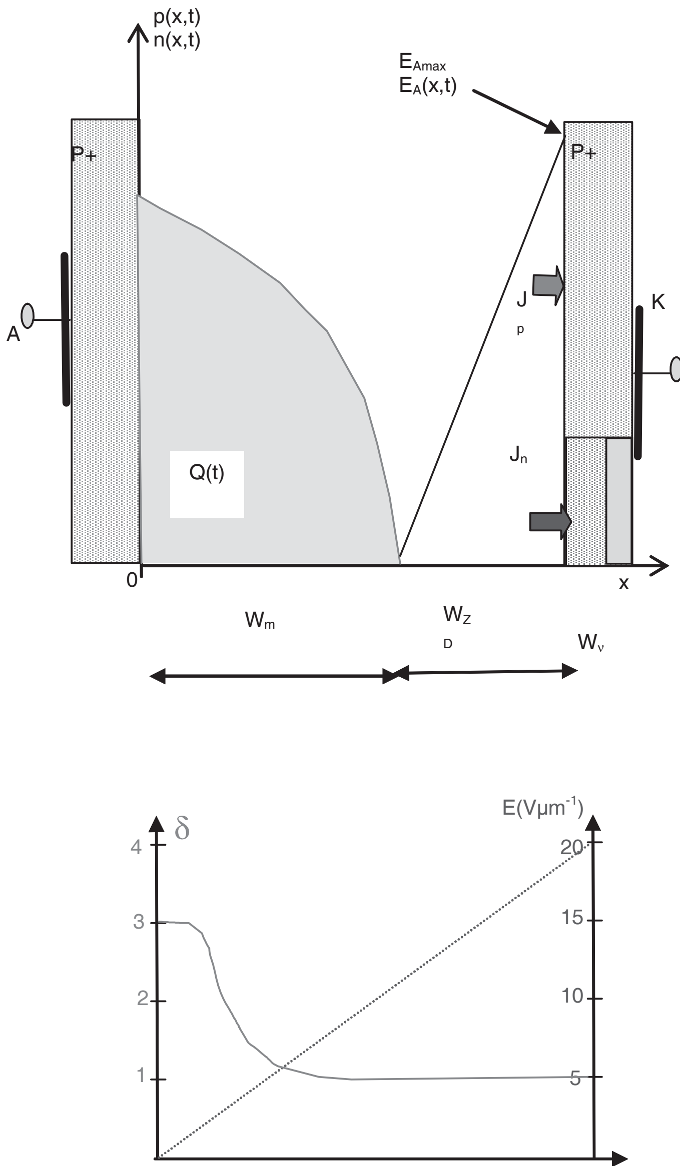


Figure 2.31. *Simultaneous occurrence of high voltage and large current in the drift zone*

We can see that β_{PNPdyn} is a determinant factor in the avalanche effect due to high current, influencing the effect in three ways:

– Hole current density is equal to electron density, $\beta_{PNPdyn}= 1$: therefore, no dynamic avalanche affects the electric field.

– Hole current density is higher than the electron current density, $\beta_{PNPdyn} > 1$. Field gradient increases with current. For a given V_{AK} voltage, when the current density increases, E_{Amax} becomes larger. Avalanching phenomenon occurs when E_{Amax} raises the silicon critical field, for example at 20 V.cm^{-1} for $N_D = 10^{14}$.cm^{-3}.

– Hole current density is less than the electron current density, $\beta_{PNPdyn} < 1$: field gradient decreases with the current, so no dynamic avalanching occurs.

Short circuit is an important constraint for IGBT dynamic avalanche. Figure 2.32 shows the short circuit waveforms of a 1,200 V, 25 A NPT-IGBT, when the load circuit V_{AK} imposes $V_{AK} = V_{SC}$, and the current is fixed by the IGBT, formulated by:

$$J_{SC}(t) = J_n(t) + J_p(t) = \frac{K^*_p}{2}(V_{GK} - V_{th})^2 + J_p(t)$$

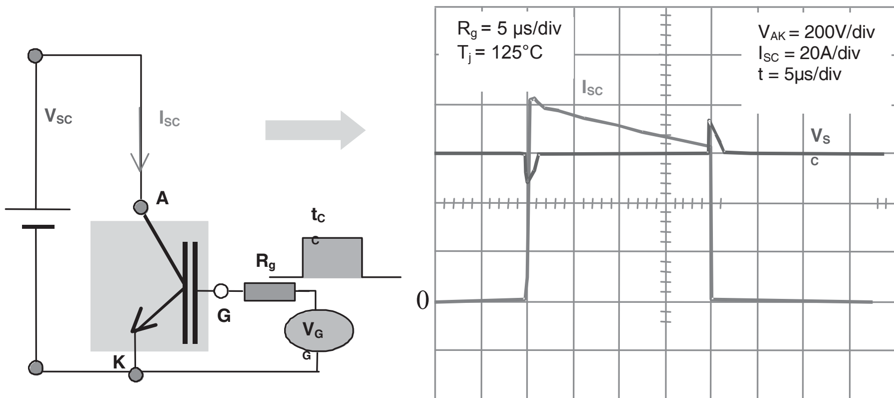


Figure 2.32. *Short circuit waveforms for a 1,200 V, 25 A NPT-IGBT*

Electron current part, $J_n(t)$, is established and rises to its maximum almost instantaneously when the short circuit occurs, because it follows the $V_{GK}(t)$ voltage. It then decreases with the short circuit because of the increase in temperature, due to losses. Hole current is established slowly, because it follows the speed of storage of charges. So, the short circuit current is, at the beginning, mainly an electron current, and, in the following of the short circuit, the hole current increases until the short circuit current is established. Despite all of this, the short circuit current slightly decreases with time: hole current cannot compensate for the decrease due to the temperature of electron current.

Dynamic avalanche study, in the short circuit case, consists of determining the maximum short circuit current density that the IGBT can sustain with a given V_{SC}. For that, β_{PNPdyn} must be determined as precisely as possible, because dynamic avalanche is completely dependant on it. However, β_{PNPdyn} varies with time, and knowledge of hole current evolution during short circuit is required. One hypothesis considers that the modulated region W_m is entirely at high level, and that charge distribution is a decreasing function. According to this hypothesis, hole current density is:

$$J_p(t) = \frac{J_n(t)}{b} - qD(1+\frac{1}{b}) \cdot \frac{dp(x,t)}{dx} > \frac{1}{b} J_n(t)$$

In this case, β_{PNPdyn} is necessarily higher than 1/b, which gives a hole current compulsorily higher than $I_{SC}/(1+b)$, or 25%. I_{SC}. If the short circuit is turned off by a quick drive, this hole current will be found in the current tail at switch-off.

By experience, in the short circuit conditions specified by manufacturers, this current is not really seen. It could be possible with a high PNP gain in a PT-IGBT with a short circuit voltage close to the maximum voltage. This means short circuit dynamic gain, β_{PNPdyn}, is much lower than 1/b, and the previous hypothesis is not always usable. It is necessary to get a more accurate model. For example, the modulated region may be divided in two regions: a high level first one close to the anode, and a low level second one close to the space charge.

Instead of determining β_{PNPdyn}, it could be better to use it as a parameter. If a linear distribution for the electric field in the space charge is considered, the current density limit imposed by the avalanche, for $\beta_{PNPdyn} > 1$, is:

$$J_{A\max} \leq \frac{1+\beta_{PNPdyn}}{\beta_{PNPdyn}-1} \cdot \{ \frac{E_{Si\max}^{\;2}}{2V_{AK}} v_{ns}\varepsilon_{si} - qN_D v_{ns} \}$$

Figure 2.33 shows this limitation for two different β_{PNPdyn} gains, 2 and 1.5, with an identical doping level $N_D = 10^{14}.cm^{-3}$. With a low anode voltage, the limiting density tied to dynamic avalanche is relatively large, therefore, only the thyristor switch-off sets the maximum density, a density which is preponderant when the anode voltage is high.

Electron current flow is possible only if the channel is conducting. The limit density given by the previous equation represents a theoretical Forward Bias Safe Operating Area (FBSOA). After the short circuit switch-off, channel is opened and only a hole current (current tail) is going through the space charge; $\beta_{PNPdyn} = \infty$. Its limit density imposed by the dynamic avalanche is:

$$J_{p\max} = J_{tail\max} \leq \frac{E_{Si\max}^{\ 2}}{2V_{AK}} v_{ns}\varepsilon_{si} - qN_D v_{ns}$$

With a fast switch-off drive, J_{Dmax} may be combined with the hole current during the short circuit, thus the reverse safe operating area in short circuit, for the IGBT, may be defined (see Figure 2.33b) as:

$$J_{A\max} \leq \frac{1+\beta_{PNPdyn}}{\beta_{PNPdyn}} \cdot \{\frac{E_{Si\max}^{\ 2}}{2V_{AK}} v_{ns}\varepsilon_{si} - qN_D v_{ns}\}$$

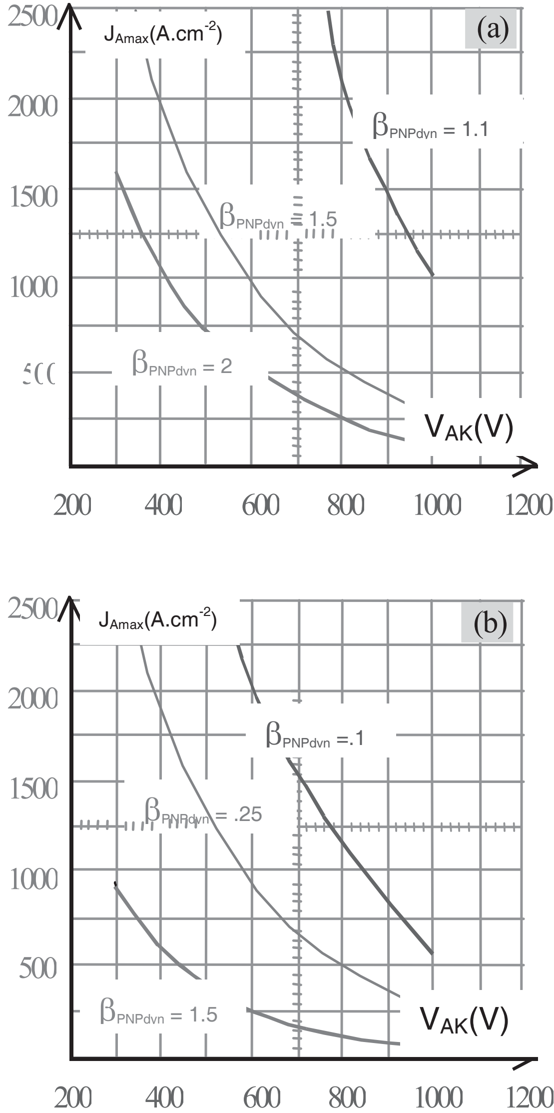


Figure 2.33. *Short circuit security areas: a) forward, for $\beta_{PNPdyn} > 1$ (no constraint for $\beta_{PNPdyn} \leq 1$); b) reverse*

If charts a) and b) from Figure 2.33 are compared, we can clearly see that the reverse safe operating area in short circuit is smaller than the area in forward short circuit.

The NPT-IGBT has a thick drift zone, which in turn gives a large W_m modulated base for the short circuit, and so a low dynamic gain $\beta_{PNPdyn} << 1$. Therefore, it can sustain large current densities under high V_{SC}, without any dynamic avalanche. Now, the PT-IGBT, with a thin drift zone, has a thin modulated base, and is weaker than the previous one. So, its β_{PNPdyn} gain is larger, and its reverse safe operating area in short circuit is smaller. In Figure 2.33, the β_{PNPdyn} gain is assumed to be constant versus short circuit voltage V_{SC}. This hypothesis is good for the NPT-IGBT thanks to its thick drift zone. For the PT-IGBT, the β_{PNPdyn} gain increases with the short circuit voltage. Accordingly, its short circuit reverse safe operating area is smaller, as seen in Figure 2.33. Inside this area, as with MOSFET, the maximum short circuit time t_{CC} only depends on silicon temperature or losses.

High switch-off current, in hard switching operations on an inductive load, may also lead the IGBT to a dynamic avalanche. In contrast to the short circuit, anode current is set by the load, rather than the IGBT itself. Until the anode voltage has not reached the supply voltage. The hole density current during switching is:

$$J_p(t) = J_A - C^*_{ZD} \frac{dV_{AK}(t)}{dt} - J_{channel}(t)$$

and is maximum when the channel is opened, with $J_{channel} = 0$. Thus:

$$J_p(t) = J_A - C^*_{ZD} \frac{dV_{AK}(t)}{dt}$$

To avoid the dynamic avalanche, current density must be limited to:

$$J_{A\max} \leq \frac{E_{Si\max}^{\;2}}{2V_{AK}(t)} v_{ns}\varepsilon_{si} - qN_D v_{ns}$$

To reduce losses, a fast drive is generally used. This means the channel turns off before the supply voltage rises (see Figure 2.34). In this case, only the hole current goes through the space charge (while $J_{channel} = 0$), and the previous expression becomes:

$$J_{A\max} \leq \frac{E_{Si\max}^{\;2}}{2V_{AK}(t)} v_{ns}\varepsilon_{si} - qN_D v_{ns} + C^*_{ZD} \frac{dV_{AK}}{dt}$$

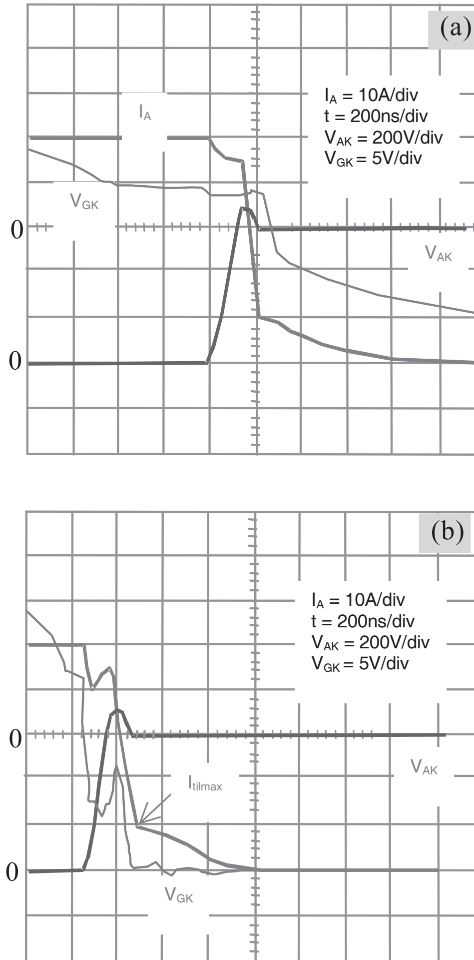


Figure 2.34. *Hard switching on inductive load switch-off: a) low drive, b) fast drive*

If the term $dV_{AK}(t)/dt$ is neglected, Figure 2.35 shows this current density versus the supply voltage. This constitutes the switch-off safe operating area for an inductive load (RBSOA). We can clearly see that this area is reduced when the anode voltage increases. However, this limitation is not entirely restrictive, due to two favorable facts:

– The rise of the anode voltage is very short because the speed $dV_{AK}(t)/dt$ with a very fast drive is very quick (tens of kV/µs): avalanching could only occur over a very short time.

– Hole current instantaneously decreases to a very low value, corresponding to the beginning of the tail, at the end of anode voltage gradient. This allows for a maximum field reduction.

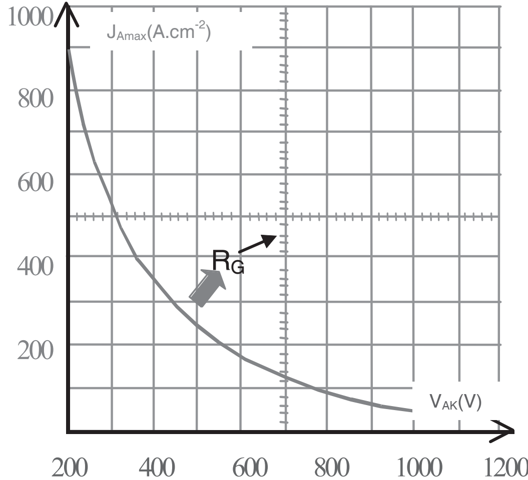


Figure 2.35. *Theoretical current limit density on an inductive load switch-off, during the anode voltage rise, with a fast drive*

Figure 2.36 shows this dynamic avalanche on a 1,200 V, 25 A NPT-IGBT. It can be seen that the dynamic avalanche occurs in a very short time. It is made at 710 V, 66 A, so for a current density of 165 $A.cm^{-2}$.

If the gate drive is slowed down, generally through R_G, the channel can continue conducting when the anode voltage is close to the Miller voltage. The more the channel is conducting, the more the area in Figure 2.35 is extended. If the channel current density becomes equal to or greater than the hole current density, this area becomes unlimited. When the anode voltage raises the supply voltage, the Miller voltage disappears and the channel is quickly opened. Electron current falls to zero and the hole current sustains the tail current. Its maximum value must not lead to dynamic avalanche. This is described by the following equation:

$$J_{tail\max} = J_{p\max} = (1+\frac{1}{b})\cdot\frac{2DQ^*}{W_m^{\ 2}} \leq \frac{E_{Si\max}^{\ \ 2}}{2V_{AK}(t)} v_{ns}\varepsilon_{si} - qN_D v_{ns}$$

If Q*tail charge density can be blended with the conduction stored charges in this expression:

$$Q^* = (\gamma_p - \frac{\beta_{PNP}}{1+\beta_{PNP}}) \cdot J_A.\tau$$

a maximum charge density in conduction, which must not be exceeded, can be deduced:

$$Q^*_{\max} \le \frac{b}{1+b} \cdot \frac{W_m^{\ 2}}{2D} \left[\frac{E_{si\max}^{\ \ 2}}{2V_{AK}(t)} \nu_{ns}.\varepsilon_{si} - qN_D \nu_{ns} \right]$$

and finally the maximum current is achieved:

$$J_{A\max} \le A_p \cdot \left[\frac{E_{Si\max}^{\ \ 2}}{2V_{AK}(t)} v_{ns} \varepsilon_{si} - qN_D v_{ns} \right]$$

with:

$$A_p = \frac{b}{1+b} \cdot \frac{1}{(\gamma_p - \frac{\beta_{PNP}}{1+\beta_{PNP}})} \cdot \frac{1}{2\tau D} \left[W_\nu - \sqrt{\frac{2\varepsilon_{si} V_{AK}}{qN_D}} \right]^2$$

This A_p coefficient is the ratio between the conduction current density and the tail maximum density. It must be greater than one, the highest possible value being preferred.

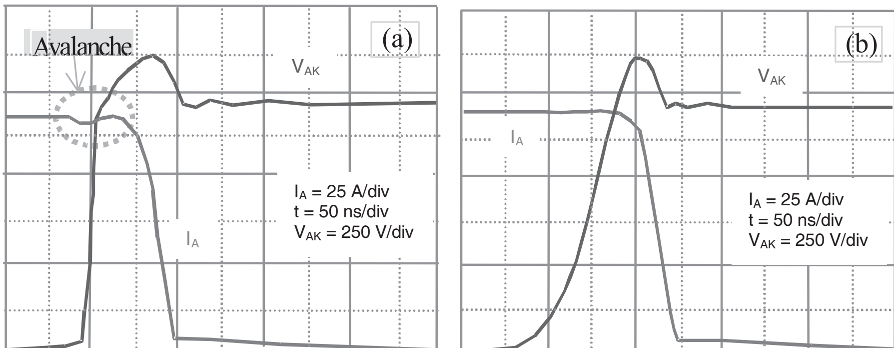


Figure 2.36. *Dynamic avalanche during hard switching -off on an inductive load: a) very low R_G with avalanche; b) high R_G without avalanche*

For this to occur, four parameters must be optimized: injection coefficient γ_p, static gain β_{PNP}, charges lifetime τ, and drift zone thickness W_ν. For example, γ_p and τ may be reduced, while β_{PNP} and W_ν may be increased, but as a drawback for static performances. Figure 2.37 shows two curves formed from the following numerical values:

$$\gamma_p = 0.4,\ W_\nu = 220\mu m,\ \beta_{PNP} = 0.4,\ \tau = 10\mu s,\ N_D = 10^{14}.cm^{-3}$$

$$\gamma_p = 0.4,\ W_\nu = 120\mu m,\ \beta_{PNP} = 0.4,\ \tau = .5\mu s,\ N_D = 10^{14}.cm^{-3}$$

The current density allowed by the dynamic avalanche decreases when the voltage increases, this limitation is more severe when the drift zone is at its narrowest (in the case of PT-IGBT). Current tail evolution is slower when the voltage increases. Therefore, avalanche, if it is possible, can spread out. Figure 2.37 shows the switch-off safe operating area on an inductive load (RBSOA).

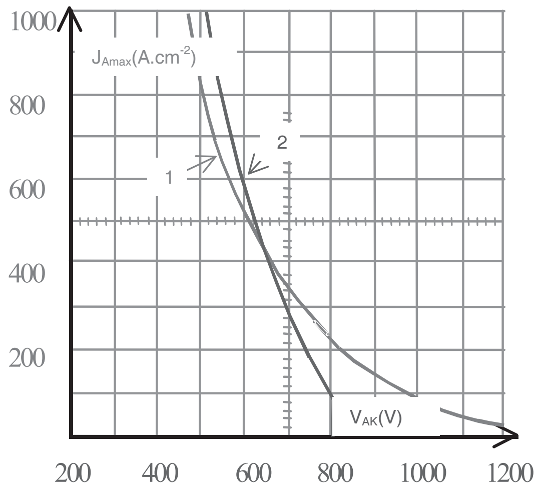


Figure 2.37. *Current density limit tied to the dynamic avalanche, at switch-off, on an inductive load*

In this section, theoretical density limits were studied versus V_{AK} voltage, following two criteria: parasitic thyristor switch-on; and dynamic avalanche, by overpass of the critical field limit. They are very complex phenomenons making their study quite difficult. Some results were shown and experiments confirmed them to be at least a tendency. IGBT are weaker than MOSFET, in over-constraint operations, due to the hole current. Now, the portion of hole current in the total

current is less inside the NPT-IGBT than the portion inside the PT-IGBT: this means NPT-IGBT are stronger in over constraint operations. Parasitic thyristor switch-on occurs at high current density; therefore it cannot be achieved if the gate voltage is maintained under the specified value, except in the case of a high transconductance parameter, K_p. The reverse safe operating area is the main limitation for short circuit current density. During short circuit, or during inductive load switch-off, the reverse safe operating area becomes smaller and smaller when the anode voltage V_{AK}, the static gain β_{PNP}, and the dynamic gain β_{PNPdyn} increase.

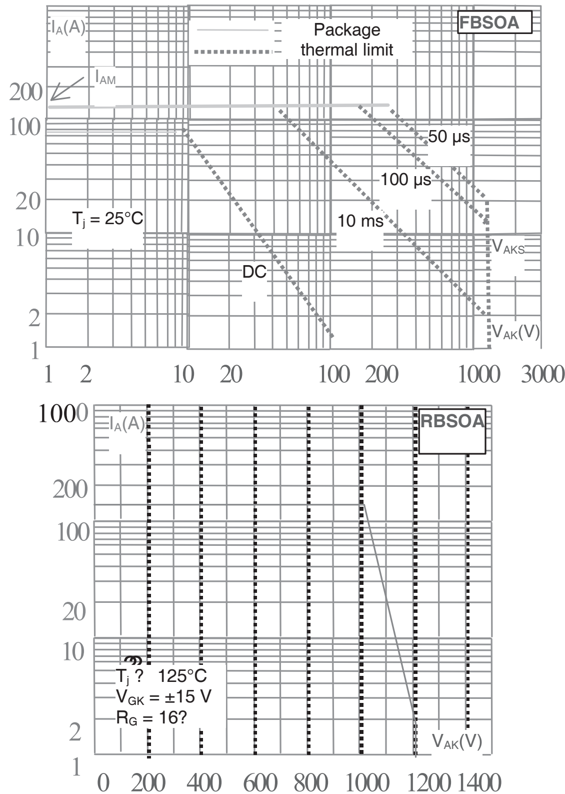


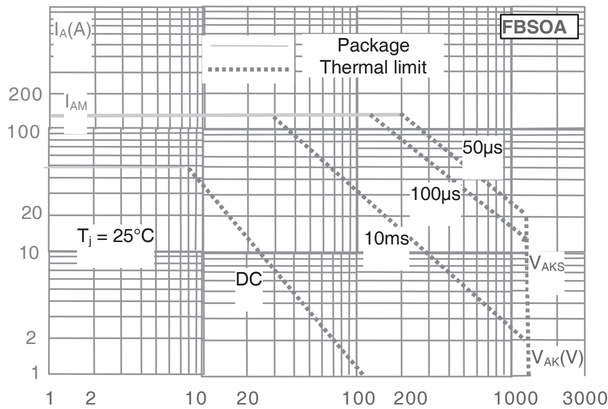
Figure 2.38. *1200 V, 75 A PT-IGBT*

2.8.3. *Manufacturer's specified safe operating areas*

All manufacturers give, for the over-constraint operations, a forward safe operating area, FBSOA, and a reverse safe operating area, RBSOA (or SSOA). Inside theses areas, current density is much lower than what was seen in the

previous chapter. The main explanation for this difference is that in the former study only physical criteria were used, while thermal and assembly constraints were forgotten. As with the I_{DM} MOSFET in the manufacturer data sheets, a maximum pulsed current I_{AM} is set, by case temperature, and it is around two to four times the operating current. Figures 2.38 and 2.39 show safe operating areas for a PT-IGBT and an NPT-IGBT, with 1,200 V, 75 A ratings. The PT-IGBT reverse safe operating area is restricted over 1,000 V, while, for the NPT-IGBT, it remains quite rectangular. These areas show three types of constraints:

– maximum sustaining Voltage V_{AKS} (V_{CES});
– junction thermal limit (around 150°C);
– maximum current I_{AM}(I_{DM}), mainly set by the internal connections.



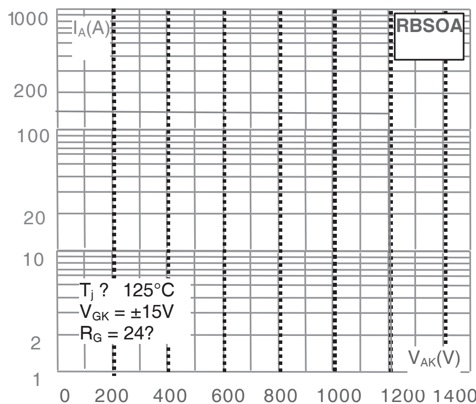
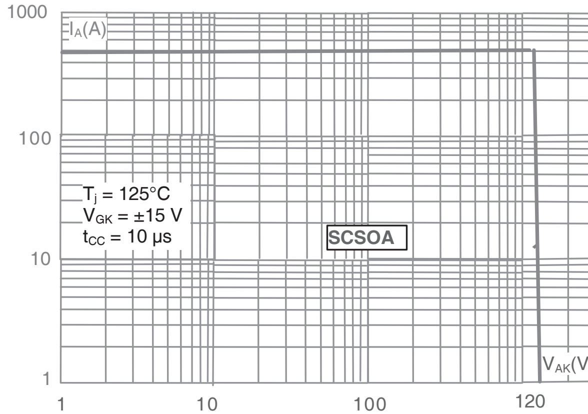


Figure 2.39. *1,200 V, 75 A NPT-IGBT*

For the short circuit, the main parameters are: initial temperature, drive voltage V_{GK} and short circuit duration t_{sc}. Most of the specifications give a maximum short circuit duration, t_{sc} = 10 µs, with an applied voltage V_A (or V_{CC}) between 50% and 70% of V_{AKS} (or V_{CES}), with a case temperature of 125°C, and a drive voltage V_{GK} = ±15 V. Several manufacturers also give a Short Circuit Safe Operating Area (SCSOA). Figure 2.40 shows two examples.



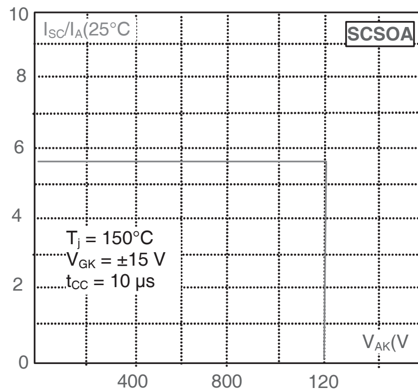


Figure 2.40. *Short circuit safe operating areas for NPT-IGBT, 1,200 V, 75 A and 25 A*

2.9. Future of IGBT

2.9.1. *Silicon evolution*

All devices under 1,500 V are built with epitaxial wafers. For IGBT, with voltages between 600 V and 1,500 V, and with a P+ substrate, this is difficult because substrate thickness is more than 100 µm, which means a large hole injection. The manufacturer needs to make a lot of particular operations in order to control the stored charges, such as N+ buried layer and electronic irradiation. For a high voltage device, this is easier to achieve utilizing a technical process called "float zone" (FZ), a thick N- substrate (10V by micron), which will be the drift zone, can be used, and the IGBT anode is made by back P+ diffusion or implantation. Today, for IGBT voltages under 2,000 V, thin wafer can be used, which allows for good control of drift zone thickness and the P+ anode diffusion layer, thus limiting the use of irradiation. Thin wafers also allow much better V_{AKsat} control, this being the main parameter for controling losses in a high current IGBT (see Figure 2.41).

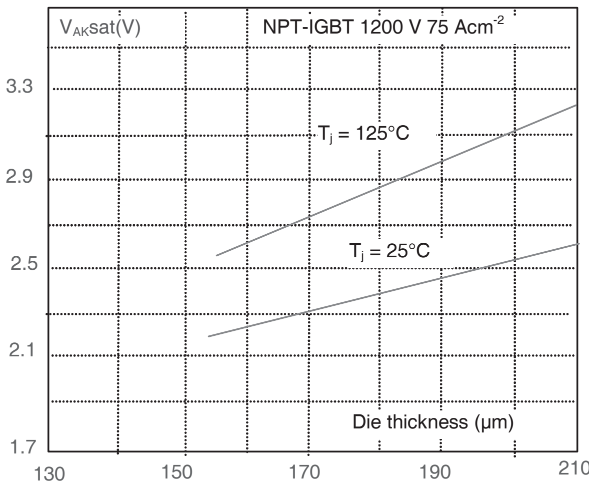


Figure 2.41. *Voltage drop versus die thickness*

Figure 2.42 shows all the IGBT technological evolutions, beginning around 1990. First, was the NPT (non punch through) technology with an epitaxial N- drift zone, and a die thickness around 300 µm, less and less used today. Second, came the PT technology, starting with the FZ technology (thin wafer for low voltage devices). This was the cheapest technology, being without N layer and irradiation, and also less sensitive to temperature. Finally, came "soft punch though" technology, again

with a buried N layer, however, this time with a good compromise between switching speeds and drop voltages, V_{AKsat}.

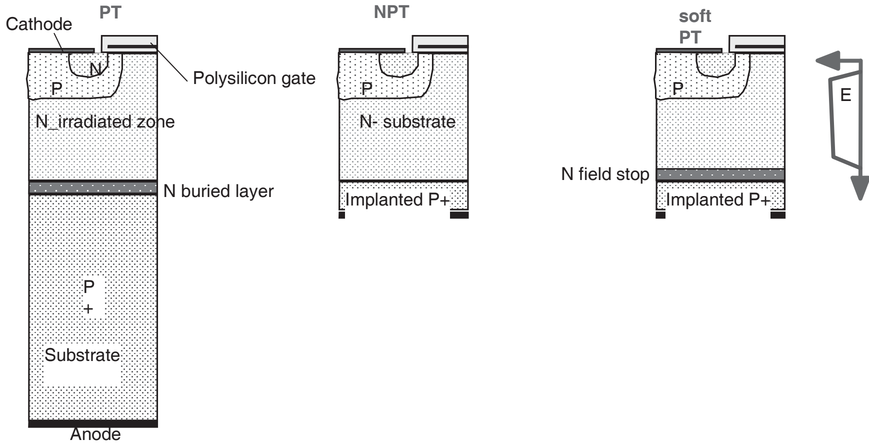


Figure 2.42. *The three IGBT technologies with the same scale, for low voltage devices (600 V to 2,000 V)*

2.9.2. *Saturation voltage improvements*

During the conduction state, electron injection is significant, so the channel resistance must be as low as possible. The solution is very well known: increase the cell number or, today, use the "trench gate technology" shown in Figure 2.43.

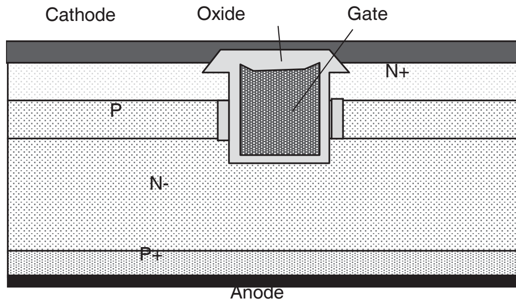


Figure 2.43. *Trench gate technology*

Saturation voltage can also be improved by using an old technology, used for GTO devices: non-connection for several gate digits. This way, the concentration of holes in the upper part of the IGBT is increased. This technology is called “IEGT: injection enhancement gate transistor”, and can be seen in Figure 2.44.

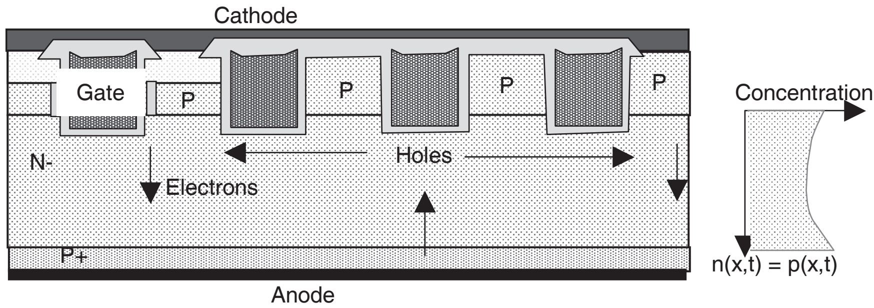


Figure 2.44. *IEGT technology*

This technology allows for an increase of current density by a factor of ten, for the same V_{AKsat}, in high voltage IGBT devices. From this same idea, Hitachi uses a technology called “hole barrier” (HiGT): this barrier consists of a N diffusion close to the Pwell. It stops the holes in this layer, making it highly modulated and lowering the saturation voltage (see Figure 2.45).

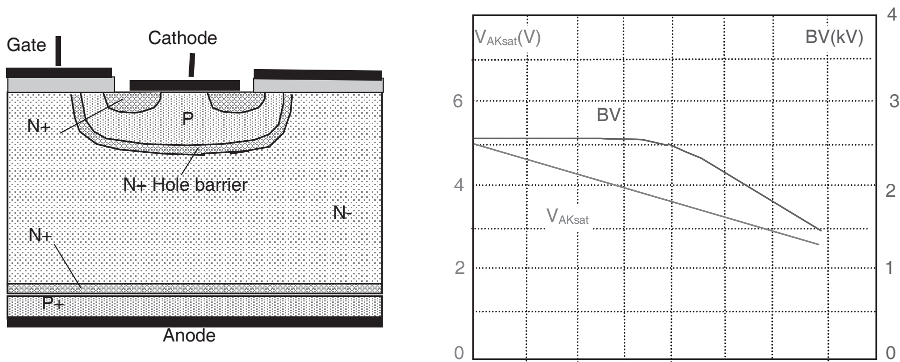


Figure 2.45. *HiGT technology*

2.10. IGBT and MOSFET drives and protections

2.10.1. *Gate drive design*

MOSFET or IGBT have combined input impedances: first a fixed capacitance made by the internal oxide between emitter and gate (or gate and cathode), and second a variable capacitance between gate and drain (or anode). They are non-linear, depending on sustained voltage and maximum current. The main design compromise is: a fast drive in order to reduce switching losses, or a slower drive to account for parasitic noises (EMC). Anyway, the drive loop must have a very low parasitic inductance to allow for both a fast drive and very low parasitic oscillations. After that comes the choice of R_G. It must be as low as possible to avoid any Miller capacitance drawback, but high enough to control the device speed. In terms of designing the gate drive, the chart of gate charge versus gate voltage is helpful (see Figure 2.13).

Switching time is $t = Q_G/I_G$, where Q_G may be divided into three parts (see Figure 2.46):

– Q_{GS} stored charges in C_{GS}, before the Miller capacitance, given by the charges produced by the gate on the upper part of the drain when $V_{GD} = 0$,

– Q_{GD} stored charges during the "plateau",

– and $Q'_{GS} + Q'_{GD}$ charges, to charge the Miller and the geometrical capacitances in series.

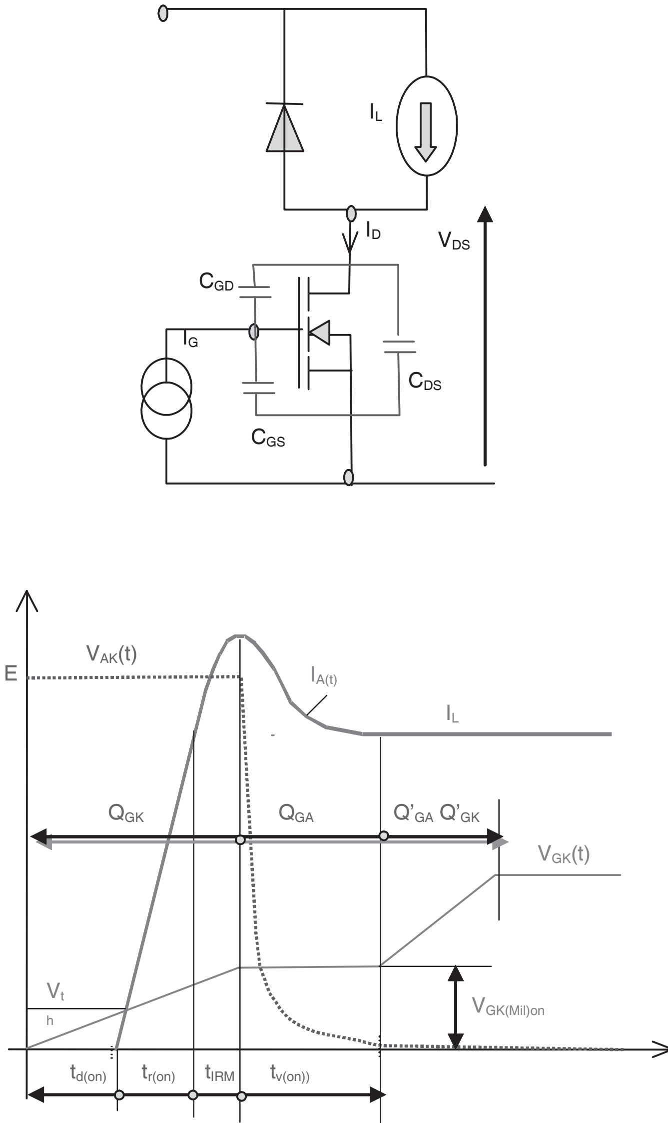


Figure 2.46. *Switch-on for an inductive load*

The Miller effect depends on switching conditions. Switching a higher current and a higher voltage increases the Miller effect (see Figure 2.47).

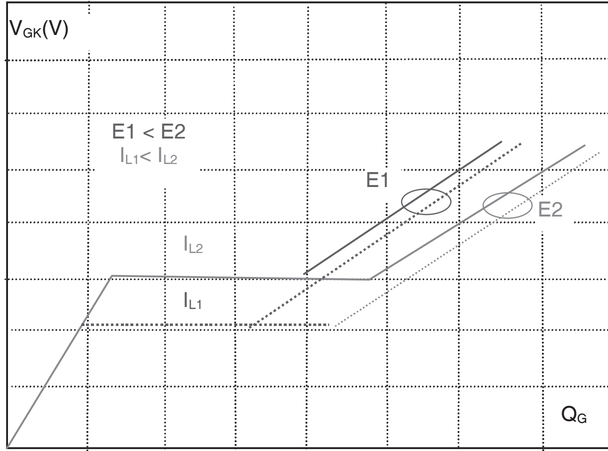


Figure 2.47. *Gate charge versus loads*

For instance, if the gate charge of the MOSFET shown in Figure 1.30 is considered: total charge quantity Q_G is 64 nC, for a gate voltage of 12 V, in a power circuit with a V_{supply} of 400 V and current of 8 A. To get to the end of the Miller effect, Q_{GS} + Q_{GD} are around half, so 32 nC. The gate peak current is:

$$I_{G\max} = \frac{Q_{GS} + Q_{GD}}{t_{d(on)} + t_{r(on)} + t_{IRM} + t_{v(on)}} = \frac{Q_{GS} + Q_{GD}}{t_{on}}$$

For a switch-on time t_{on} of 100 ns, a gate peak current of 0.32 A is needed.

For a working frequency of 100 kHz, the drive power is:

$$P_G = Q_G.V_{GS}.F = 64.10^{-9}.12.10^{5} \approx 77 \text{ mW}$$

This is very low compared to the power controlled: 400 V with 8 A.

2.10.2. *Gate drive circuits*

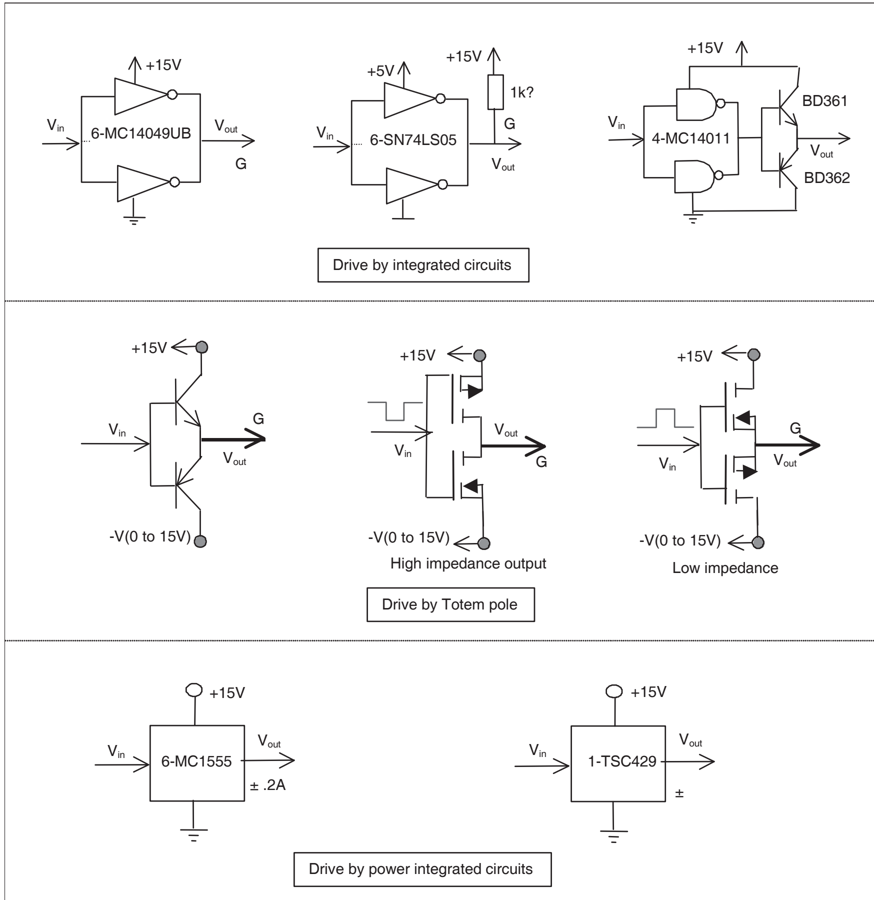


Figure 2.48. *MOSFET and IGBT discrete drives*

MOSFET and IGBT gate drives are the same. Only for high current IGBT might it be better to use $V_G = \pm 15$ V in order to protect the device against the counter reactive drawbacks of the Miller capacitance, and against high dV/dt. There are numerous gate drive circuits with a choice of criteria:

– speed with working frequency;

– load current driven;

– negative voltage drive; and

– galvanic insulation.

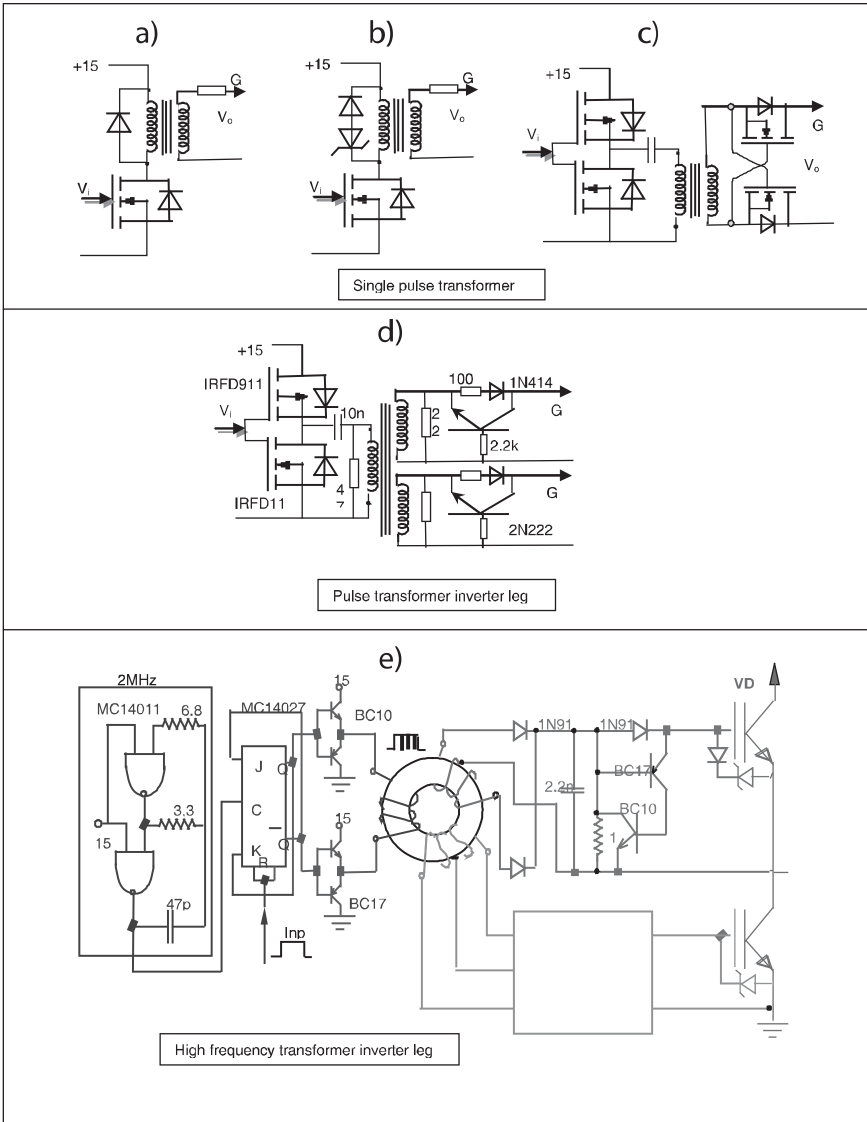


Figure 2.49. *MOSFET and IGBT transformer drives*

Figure 2.48 shows some classical drive circuits, made of various low power drive components. When integrated circuits are used, parallel connection of several integrated circuits is required most of the time (sometimes in a same package), in order to produce enough current to efficiently drive the MOSFET or IGBT. TTL

circuits are faster than the CMOS circuits, but their output voltage is, most of the time, too low (≤5 V) to directly drive the power device, but their open collector output allows for a direct connection to the auxiliary source (10 V to 15 V), through a "pull up" resistor, in order to obtain enough energy to drive the power device (this product family is normally used to drive low power devices). The resistance must be quite high in order to keep the TTL internal current low enough. This reduces the switch-on switching time.

The discrete drive circuit family is mainly represented by three "totem pole" types: first, with complementary bipolar devices; and second, with complementary MOS devices. The third can be divided into two other types: one with the emitter connected for a low impedance output, and the other with the drain connected for a high impedance output. It is very easy to drive these circuits with only one signal, because each of them excludes the other one when it is in the on-state. The drive reference could be the common connection, but due to the MOS or bipolar voltage drop, it is difficult to be less than the power device V_{th}, and it may be better to use a negative source for the bottom device connection. Some "push pull" drives also exist, made of MOS or bipolar. They are similar to the previous ones, however, they use the same polarity devices, and so need two opposite drive signals. Totem pole circuits are commonly used as they are very simple and efficient. Sometimes, they are used at the output of integrated circuits to directly drive the power device. Some power integrated circuits also exist to drive the power MOS or the power IGBT, with an output gate current of several amperes peak.

At the beginning, a lot of designers tried to use pulsed transformers (see Figure 2.49). The main advantage of these circuits is the galvanic insulation, which allows a lot of possibilities, mainly for floating references. It can also manage the drive signal, and gives enough energy to the gate.

Two basic elements must be taken into account for the pulsed transformer. On the primary side, applied voltage (assumed constant), multiplied by the time, must be under the magnetic saturation of the magnetic circuit. On the secondary side, conduction time, multiplied by the positive voltage, must be equal to the negative voltage, multiplied by the off-state time. This makes a strong limitation on the duty cycle. A lot of "tricks" are used to overcome this limitation. In Figure 2.49a, the basic principle is shown: if a zener is added (see Figure 2.49b), the duty cycle can be larger, however, it remains limited to 50% if $Vz \leq 15$ V. Figures 2.49c and 2.49d show two possible improvements for the duty cycle: adding a small capacitor on the primary side of the transformer (to avoid any transformer saturation); and using a memory circuit on the secondary side, which keeps the stored energy on the capacitance when the pulsed drive signal disappears. Nevertheless, transformer design is still difficult, due to the parasitic capacitances between transformer coils, which limit the dV/dt. Figure 2.49e shows a solution which provides a large duty

cycle with good immunity against dV/dt, by using a high frequency ring transformer. This allows few transformer turns, and so a low parasitic capacitance. A high frequency clock (for instance at 2 MHz) is cut off by the drive frequency (of for instance 100 kHz), in such a way that the transformer is designed for a 2 MHz frequency, while the secondary side of the transformer integrates and memorizes the drive signal.

Floating drive circuits are mainly requested for inverter leg drives, while the upper switch has a floating reference between zero volt and the applied voltage.

Combined with transformers, opto-electronic devices are good solutions. They make a very good insulation between drive and output. Figure 2.50a shows a basic opto-drive circuit. The optic fiber, in Figure 2.50b, has the same function as the transformer, however, if this optic fiber passes through a shield a good EMI insulation is obtained. Figures 2.50c and 2.50d show two double opto-drive circuits for large IGBT or MOS devices.

Figure 2.50e shows a voltage doubler (or charge pump) drives the upper side of the inverter leg, but this design is mainly limited to low power voltage and is quite slow (automotive applications by example).

Figure 2.50f is a resonant drive circuit. Resonance occurs between the input gate inductor and the internal MOS capacitances. This design provides an overvoltage, between 10 V and 15 V, from an auxiliary source of only 5 V.

A non-galvanic-insulated upper side drive circuit, may be created with two complementary drive devices (see Figure 2.51a). This design produces large duty cycles and is easy to make. The main limitations are the need for an auxiliary voltage of 15 V, other than the power voltage, and that the drive circuit is not protected against the power voltage by galvanic insulation.

A drive circuit is commonly used today for inverter legs: the “bootstrap” drive circuit. Figure 2.51b shows the principle. The energy needed to drive the upper side is stored in the external capacitor. When the lower switch is ON, a little diode is used in series in order to avoid any reverse current when the lower switch is off. An integrated high voltage logic circuit is used to translate the drive signal from the ground to the upper side.

Figure 2.51c shows the low voltage possibility of bootstrap. As MOS Q1 and the capacitor sustain the power voltage, an emitter follower, BD361 for instance, may be added to the basic circuit.

In conclusion, many high voltage integrated circuits are available on the market, to translate the signal and to charge the capacitor. Some of these HV-ICs can drive a three-leg inverter. The duty cycle is limited, in order to let enough time to charge the capacitor.

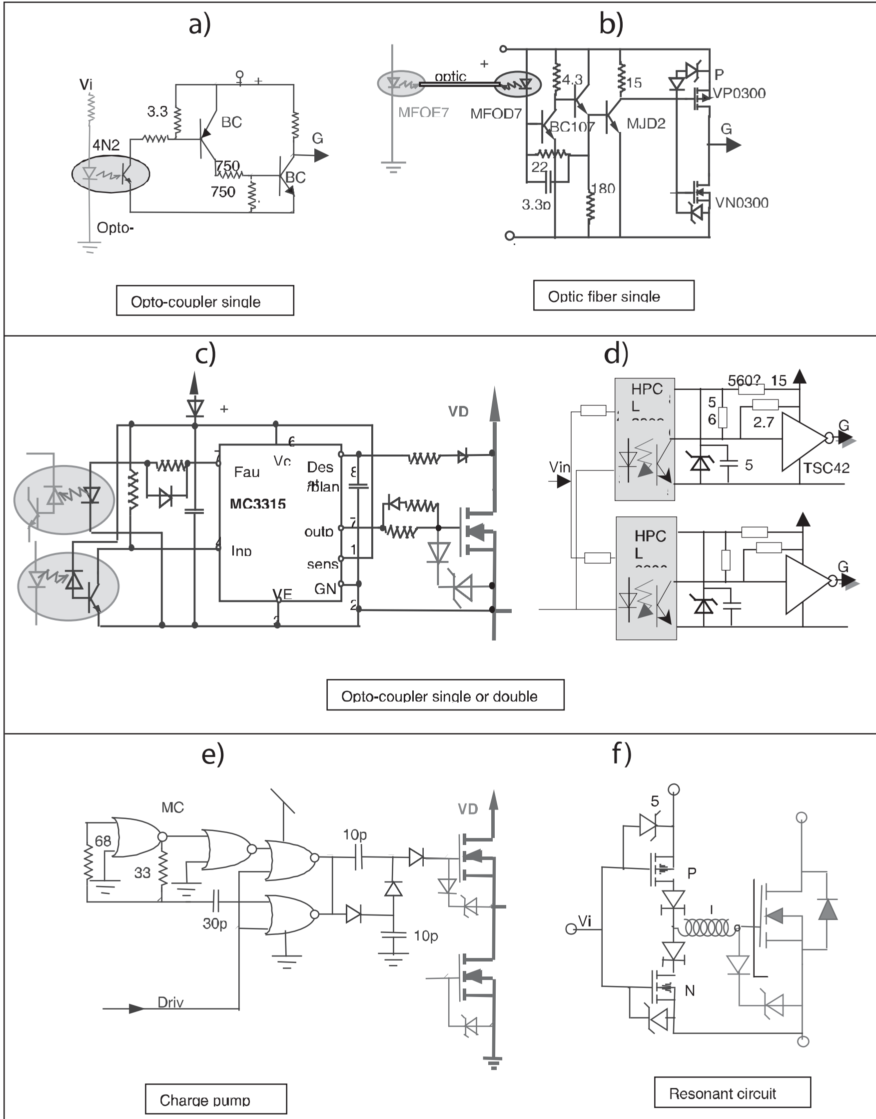


Figure 2.50. *MOSFET and IGBT special drive circuits*

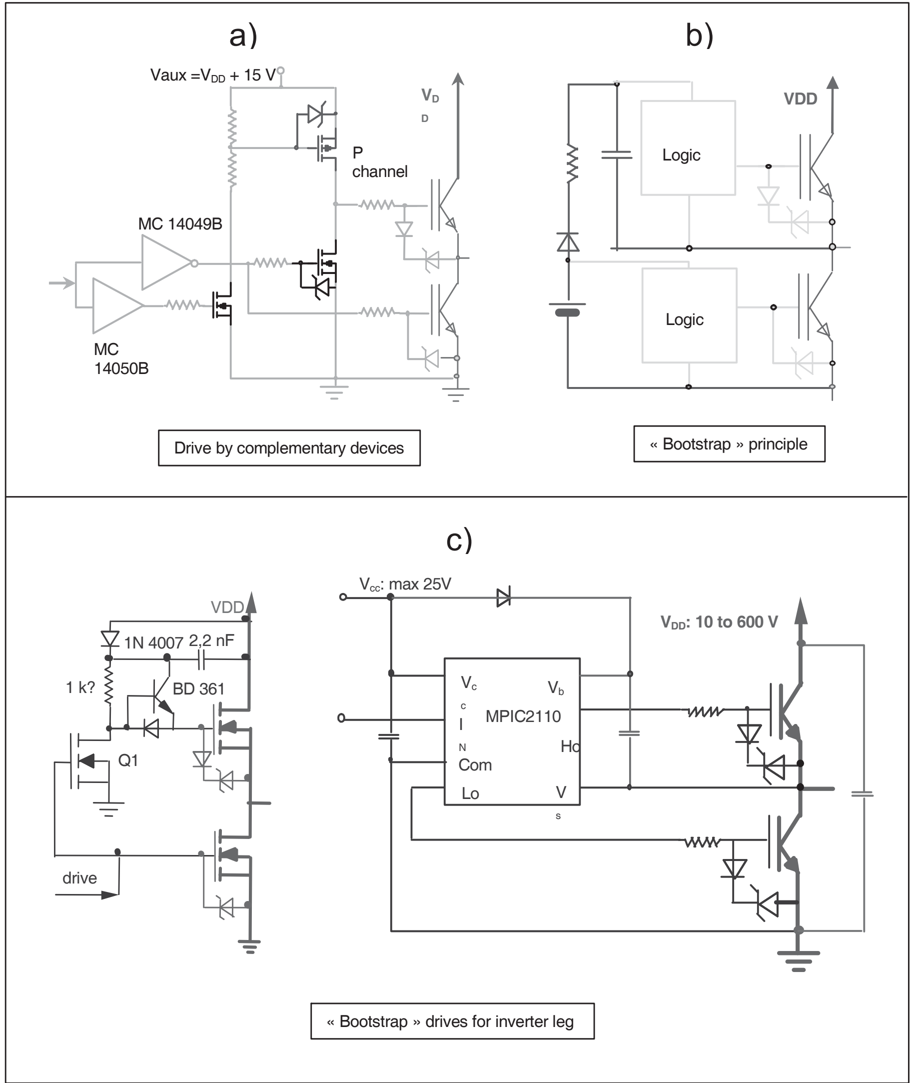


Figure 2.51. *MOSFET and IGBT upper side drive circuits*

2.10.3. *MOSFET and IGBT protections*

2.10.3.1. *Over-current protections*

Current or voltage measurements are needed, for over-current protections (see Figure 2.52). The current transformer is a very simple measurement system, however, due to the volume of the device, it is mainly used for high magnituded currents.

Voltage drop on a resistor is also a very simple idea, but this resistor must have very low resistance to have low losses, and be non inductive to avoid any ringing. This is an expensive resistor, mainly used for very low currents.

A non-dissipative solution is to measure the drain or anode voltage. Over-current on the IGBT means de-saturation and an increase of the anode voltage. A threshold comparator connected between anode-cathode of the IGBT detects this voltage and a switch-off signal can be issued.

For high current circuits, turning off the short circuit current (several thousands of amps) is very difficult, due to the high dI/dt, and overvoltage, LdI/dt. So, the best solution, when a short circuit current is detected, is to decrease V_{GSC} to a value $I_{SC} = G_{fs} \times V_{GK} \approx I(\text{rated})$, with a zener such as $Vz = V_{GSC}$. If the defect is still present after a few micro seconds (5 to 10), the system is switched off with only the rated current.

2.10.3.2. *Overvoltage protection*

The MOS or IGBT “Achille heel” is the gate oxide protection, because, with a thickness of around 100 nm and a rated voltage of 20 V, the device lifetime mainly relies upon the gate oxide stresses. So, it is mandatory to use a fast zener between gate and source or cathode (see Figure 2.52e).

MOSFET or IGBT can sustain accidental avalanches, but the lifetime of these devices is also limited by the avalanche stress. So, an avalanche diode (or a zener) is sometimes used between drain and source, or anode and cathode, to absorb the avalanche energy. The diode must be large enough to support this energy, making it an expensive device. For the same purpose, a small zener could be connected between drain and gate, or anode and gate, to drive the power device on, before the device avalanche. This will absorb the energy, not in avalanche, but in conventional operation. A standard diode must be connected in series to avoid any current running from the gate to the drain in on-state.

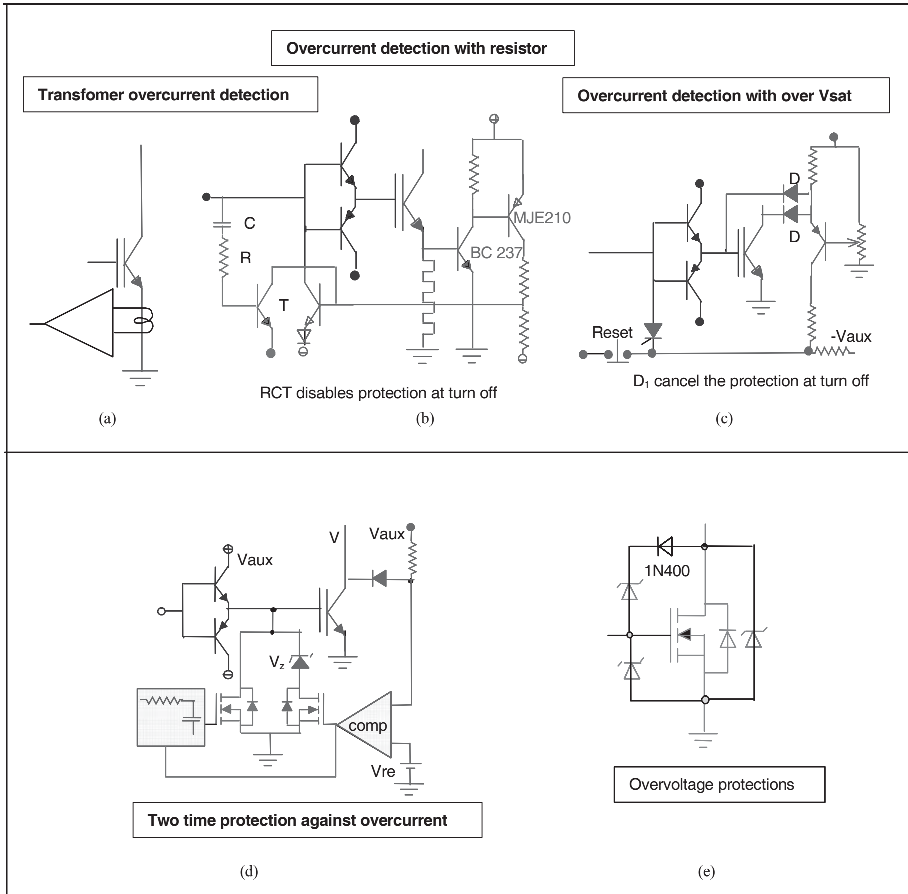


Figure 2.52. *MOSFET and IGBT over-current and overvoltage protection*

2.11. References

[ALN 98] ALNAHAR M., LI J.M., LAFORE D., "Méthode simple d'estimation de la durée maximume de court-circuit t_{ccmax} des IGBTs", *EPF, Proc*. 1998.

[ALN 99] ALNAHAR M., Comportement de l'IGBT en régime extrême, PhD Thesis, INPG, 1999.

[ALO 90] ALOISI P., CORDONNIER C.E., "L'IGBT et ses alternatives", *Onde Electrique*, vol. 70(5), 1990.

[ARN 92] ARNOULD J., MERLE P., *Dispositifs de l'électronique de puissance*, Hermès, 1992.

[BAL 87] BALIGA B.J., *Modern Power Devices*, John Wiley & Sons, 1987.

[BOS 92] BOSE B.K., "Evaluation of modern power semiconductor devices and future trends of converters", *IEEE Trans. on Industry Applications*, vol. 28(2), 1992.

[CAL 95] CALMON F., Participation à l'étude du comportement électrothermique des IGBTs, Thesis, INSAL, 1995.

[CAS 91] CASTINO G., BORGARO TORINESE, "Protecting IGBT's against short-circuit", *EPE Journal*, vol. 1(2), October 1991.

[CHA 90] CHANTE J.-P., "Eléments de physique sur le composant de puissance IGBT", *Onde Electrique*, vol. 70(5), 1990.

[CHE 95] CHEN DAN Y., GRANT CARPENTER, "Nodestructive RBSOA characterization of IGBT's and MCT's", *IEEE Trans. on Power Electronics*, vol. 10(3), 1995.

[CLA 94] CLAUDIO-SANCHEZ A., LI J.M., LAFORE D., "Behavior analysis of the IGBT in hard and soft switching modes by a soft modelling concept", *Proc. CIEP'94,* Puebla, Mexico, August 1994.

[CLA 95] CLAUDIO-SANCHEZ A., Etude comportementale des IGBTs dans les divers modes de commutation, Thesis, INPG, November 1995.

[CLE 93] CLEMENTE S., "Transient thermal response of power semiconductor to short power pulses", *IEEE Trans. on Power Electronics*, vol. 8(4), October 1993.

[ELA 97] ELASSER A., PARTHASARATHY V., TORREY D.A., "A study of internal device dynamics of punch-through and nonpunch-through IGBTs under zero-current switching", *IEEE Trans. on Power Electronics*, vol. 12(1), 1997.

[GHA 87] GHANDHI S.K., *Semiconductor Power Devices*, John Wiley & Sons, 1987.

[GOE 94] GOEBEL H., "A unified methode for modeling semiconductor power devices", *IEEE Trans. on Power Electronics*, vol. 9(5), 1994.

[GRA 89] GRANT D.A., GOWAR J., *Power MOSFETS Theory and Applications*, John Wiley & Sons, 1989.

[GRO 67] GROVE A.S., *Physics and Technology of Semiconductor Devices*, John Wiley & Sons, 1967.

[HEF 87] HEFNER A.R., BLACKBURN DAVID L., "Performance trade-off for the insulated gate bipolar transistor: buffer layer versus base lifetime reduction", *IEEE Trans. on Power Electronics*, vol. 2(3), 1987.

[HEF 88] HEFNER A.R., BLACKBURN D.L., "An analytical model for the steady-state and transient characteristics of the power insulated-bipolar transistor", *Solide State Electronics*, vol. 31(10), 1988.

[HEF 90] HEFNER A.R., "An analytical modeling of device-circuit interactions for power insulated gate bipolar transistor (IGBT)", *IEEE Trans. on Industry Applications*, vol. 26(6), 1990.

[HEF 91] HEFNER A.R., "Investigation of drive circuits requirements for the power insulated gate bipolar transistor (IGBT)", *IEEE Trans. on Power Electronics*, vol. 6(2), 1991.

[HEF 94] HEFNER A.R., “A dynamics electrothermal model for the IGBT”, *IEEE Trans. on Industry Applications*, vol. 30(2), 1994.

[HEF 95] HEFNER A.R., “Modeling buffer layer IGBT’s for circuit simulation”, IEEE *Trans. on Power Electronics*, vol. 10(2), 1995.

[HID 98] HIDEO MATSUDA, “New advanced semiconductors, from the state-of-the-art to future trends”, *PCIM*, 1998.

[INT 94] INTERNATIONAL RECTIFIER, IGBT designer’s manual, section application notes, IGBT-3, USA, 1994.

[KON 96] KONRAD S., ZVEREV I., “Protection concepts for rugged IGBT modules”, *EPE Journal*, vol. 6(3-4), 1996.

[LAS 92] LASKA T., MILLER G., NIEDERMEYR J., “A 2000 V non-punchthrough IGBT with high ruggedness”, *Solide State Electronics*, vol. 35(5), 1992.

[LEF 94] LEFEBVRE S., FOREST F., COSTA F., CHANTE J-P., “Optimisation de la commande de l’IGBT utilisé en quasi-résonance”, *RGE*, no. 2, 1994.

[LEF 99] LEFEBVRE S., MISEREY F., “Analysis of CIC NPT IGBT’s turn-off operations for high switching current level”, *IEEE Trans. on Electron Devices*, vol. 46(5), 1999.

[LET 95] LETOR R., ANICETO G.C., “Short circuit behavior of IGBT’s correlated to the intrinsic device structure and on the application circuit”, *IEEE Trans. on Industry Applications*, vol. 31(2), 1995.

[LET 97] LETURCQ P., DEBRIE J.-L., BERRAIES M.O., “A distributed model of IGBTs for circuit simulation”, *EPE’97 Proc*., vol. 1, 1997.

[LI 98] LI J.M., Comportement des semi-conducteurs de puissance dans leur environnement de commutation par modélisation douce, Mémoire d’habilitation à diriger des recherches, Aix-Marseille University III, 1998.

[MIT 94] MITSUBISHI ELECTRIC ADVANCE, *Power Electronics Edition*, vol. 66, March 1994.

[NAK 85] NAKAGAWA A., OHASHI H., “600 and 1 200 V bipolar mode MOSFET’s with high current capability”, *IEEE Trans. on Electron Devices*, vol. 6(7), 1985.

[PEN 98] PENDHARKAR S., TRIVEDI M., “Electrothermal simulation in punchthrough and nonpunchthrough IGBTs”, *Trans. on Electron Devices*, vol. 45(10), 1998.

[PEN 98] PENDHARKAR S., TRIVEDI M., “Zero voltage switching behavior of punchthrough and nonpunchthrough insulated gate bipolar transistors (IGBT)”, *IEEE Trans. on Electron Devices*, vol. 45(8), 1998.

[POR 90] PORST A., HERBERG H., MILLER G., STRACK H., “The transistor behavior in circuit with a shorted load”, *IEEE Trans. on Industry Applications*, vol. 26(4), 1990.

[RAH 95] RAHUL S. CHOKHAWALA, CATT J., KIRALY L., “A discussion on IGBT short-circuit behavior and fault protection schemes”, *IEEE Trans. on Industry Application*, vol. 31(2), 1995.

[ROG 88] ROGNE T., RINGHEIM N.A., ODEGARD B., ESKEDAL J., UNDERLAND T.M., "Short circuit capability of IGBT (Comfet) transistor", *IEEE Trans. on Industry Applications*, vol. 1, October, 1988.

[SPU 99] SPULBER O., NARAYANAN E.M.S., HARDIKAR S., DE SOUZA M.M., SWEET M., BOSE S.C., "A nouvel gate geometry for the IGBT: the trench planar insulated gate bipolar transistor (TPIGBT)", *IEEE Trans. on Electron Device Letters*, vol. 20(11), 1999.

[SZB 81] SZE S.M., *Physics of Semiconductor Devices*, John Wiley & Sons, 1981.

[SZB 85] SZE S.M., *Semiconductor Devices Physics and Technology*, John Wiley & Sons, 1985.

[TOS 93] TOSHIBA, IGBT Data, section explanation, Japan, 1993.

[TRI 98] TRIVEDI M., SHENAI K., "Investigation of the short-circuit performance of an IGBT", *IEEE Trans. on Electron Devices*, vol. 45(1), 1998.

[TRI 99] TRIVEDI M., SHENAI K., "Internal dynamics of IGBT under zero-voltage and zero-current switching conditions", *IEEE Trans. on Electron Devices*, vol. 46(6), 1999.

[UDR 99] UDREA F., CHAN S.S.M., THOMSON J., TRAJKOVIC T., WAIND P.R., AMARATUNGA G.A.J., CREES D.E., "1.2kV trench insulated gate bipolar transistors (IGBT's) with ultralow on-resistance", *IEEE Trans. on Electron Device Letters*, vol. 20(8), 1999.

[WIL 87] WILLIAMS B.W., *Power Electronics, Devices, Drivers, and Applications*, John Wiley & Sons, 1987.

[YIL 86] YILMAZ H., BENJAMIN J.L., DYER R.F., CHEN L.-S.S., VAN DELL W.P., PIFER G.C., "Comparison of the punch-through and non-punch through IGT structures", *IEEE, Trans. on Industry Applications*, vol. 22(3), 1986.